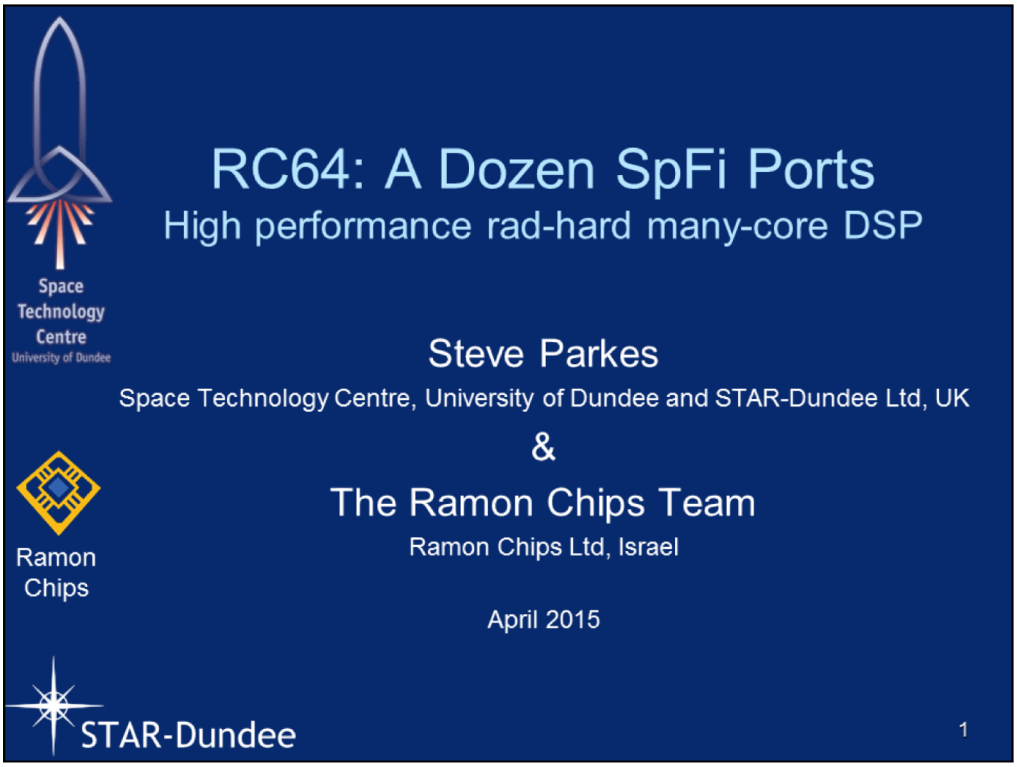
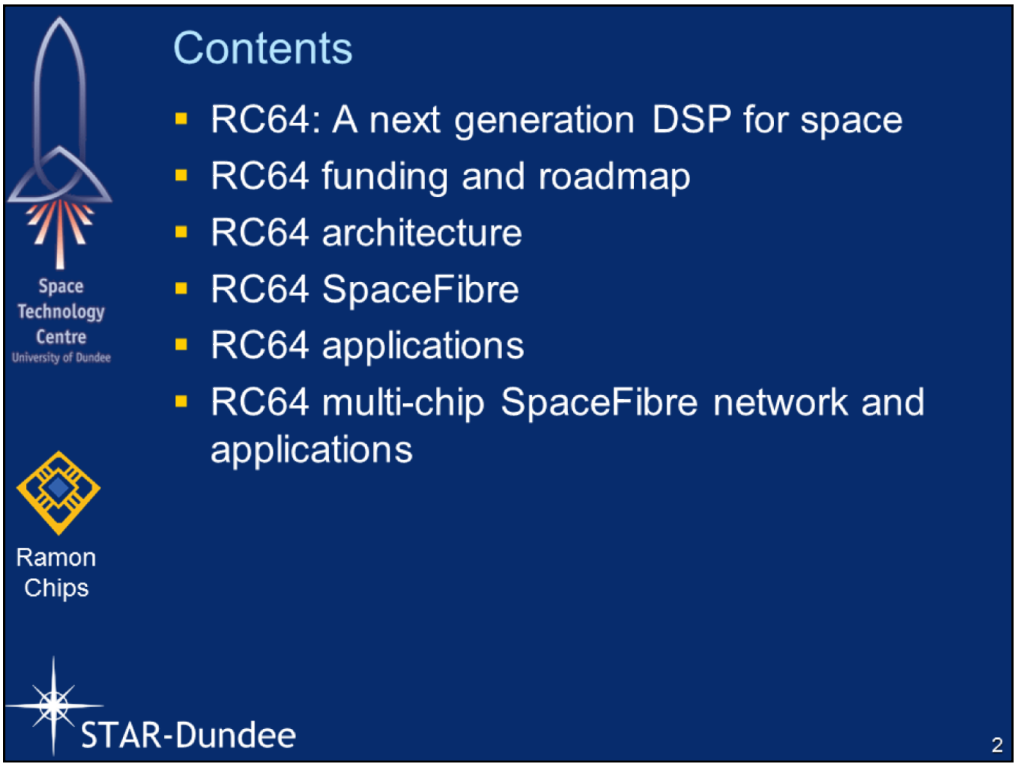

Space
Technology
Centre
University of Dundee
RC64: A Dozen SpFi Ports
High performance rad-hard many-core DSP
Steve Parkes
Space Technology Centre, University of Dundee and STAR-Dundee Ltd, UK
&
The Ramon Chips Team
Ramon Chips Ltd, Israel
Ramon
Chips
April 2015
STAR-Dundee
1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RC64 applications
RC64 multi-chip SpaceFibre network and applications
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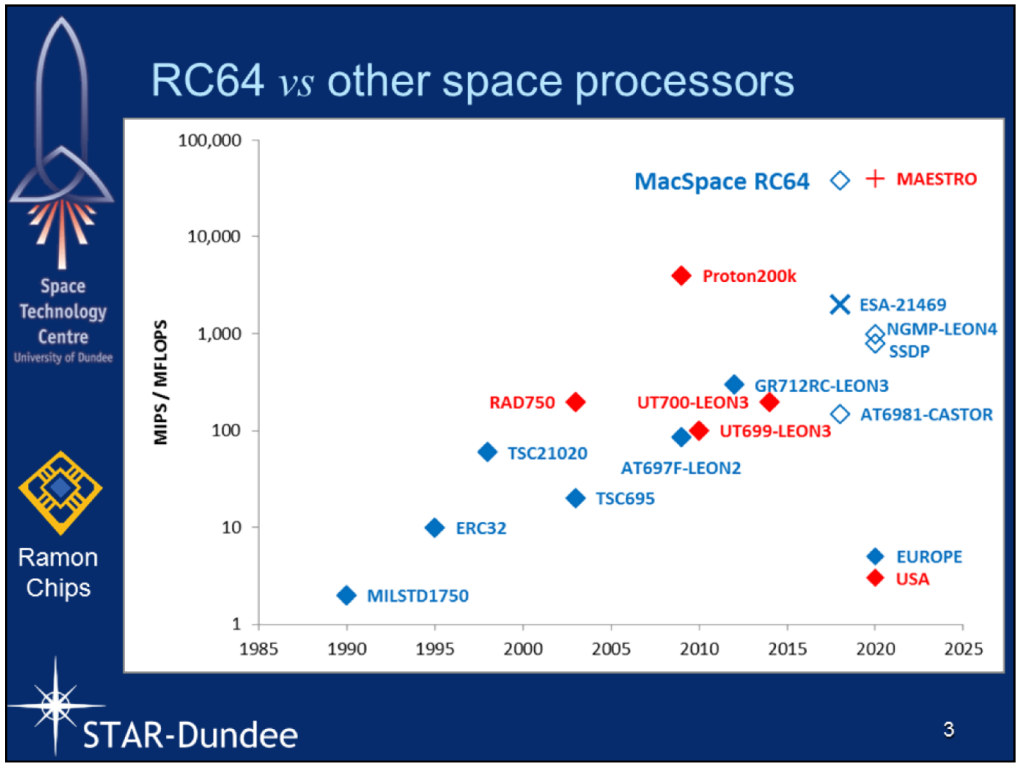
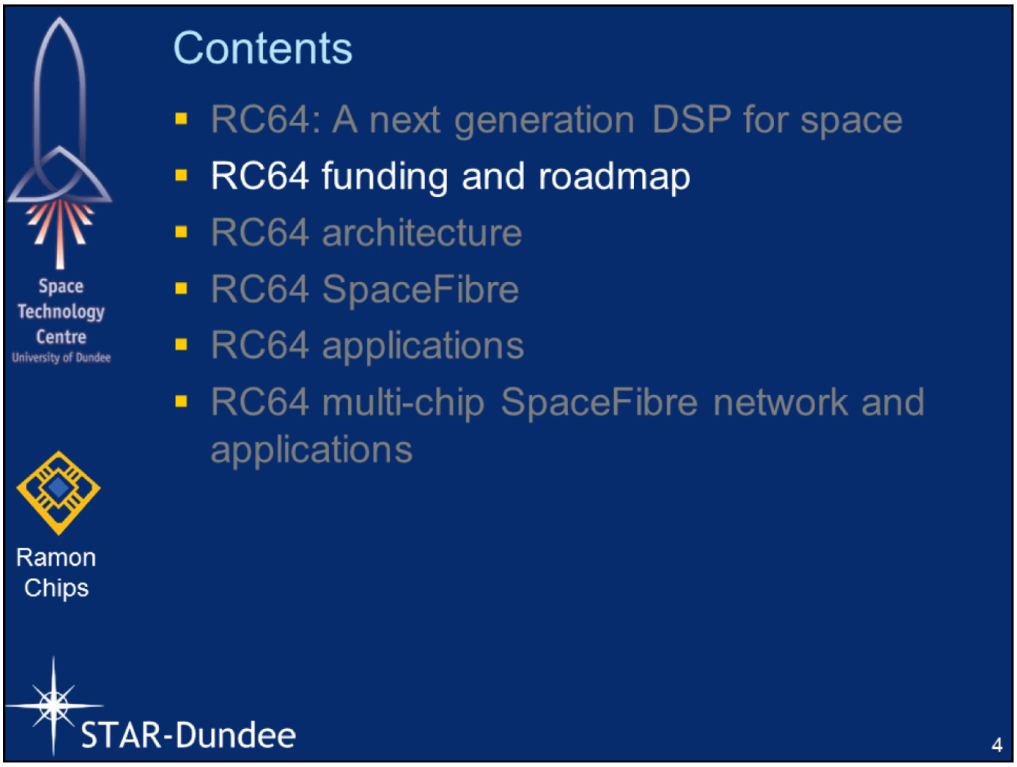


Maestro was designed by Boeing, funded by DTRA (US Government) as part of the OPERA program. It contained 49 cores from Tilera and was intended for fabrication on IBM 90nm SOI-CMOS process [Malone, MAPLD 2009]. The project seems to have ceased in 2011 and there have been no publications since then on any progress.

ESA-21469 was an attempt by ESA (NGDSP effort) to buy license for the 21469 single-core DSP from Analog Devices (USA) and convert it into a space ASIC in Europe. The project was aborted due to very high cost of the license [analyzed by John Franklin, Astrium-UK as described on ESA DSP Day in 2012 and explained in presentations by Dr. Roland Trautner in ESA DSP Day 2014].

Proton 200k is a USA-made card with TI TMS320C6713 running as “temporal TMR” [Czajkowski & McCartha, “Ultra Low-Power Space Computer Leveraging Embedded SEU Mitigation,” IEEE Aerospace, 2003].

SSDP (Scalable Sensor Data Processor) is ESA-funded project by TAS-E and Recore to create a rad-hard DSP. Its first generation will include two Recore DSP cores and implement in 180nm CMOS using IMEC DARE library [DSP_Day_2014_-_SSDP_Development_Status_TASE.pdf, ESA DSP day, Sept 2014]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RC64 Funding

- Israel Space Agency
  - $10M, 2013-2018, support silicon and environment
- Israel MoD R&D Directorate
  - $2M, 2013-2018, support applications
- EC FP7 project MacSpace
  - 2.5M€, support collaboration and applications
    - Thales Alenia Space Italia (space, IT)
    - DSI (digital systems, DE)
    - Technical University Braunschweig (algorithms & SW, DE)
    - PRESTO Engineering (testing, FR)
    - CEVA (DSP cores, IR)
    - Ramon Chips (RH ASIC, IL)
    - ARTTIC (Mngmt, FR)

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EU FP7 VHiSSI Experimental SpaceFibre ASIC

UNIVERSITY OF DUNDEE

STAR-Dundee

RAMONchips

ihp innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

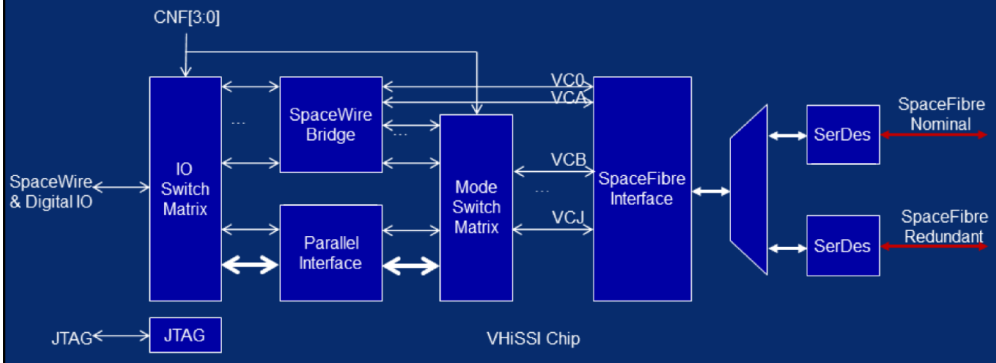
ACE ic ASIC Design House

ASTRIUM AN EADS COMPANY

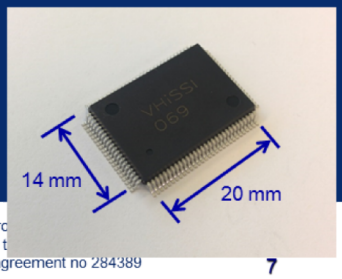
SYNERGIE CAD INSTRUMENTS

6

VHiSSI Architecture



- Fully integrated SpaceFibre interface
- 2.5 Gbits/s
- Small size, 20 x 14 mm package
- Radiation tolerant
- Prototypes in 2014



This project has received funding from the Euro
Seventh Framework Programme for research, t
development and demonstration under grant agreement no 284389

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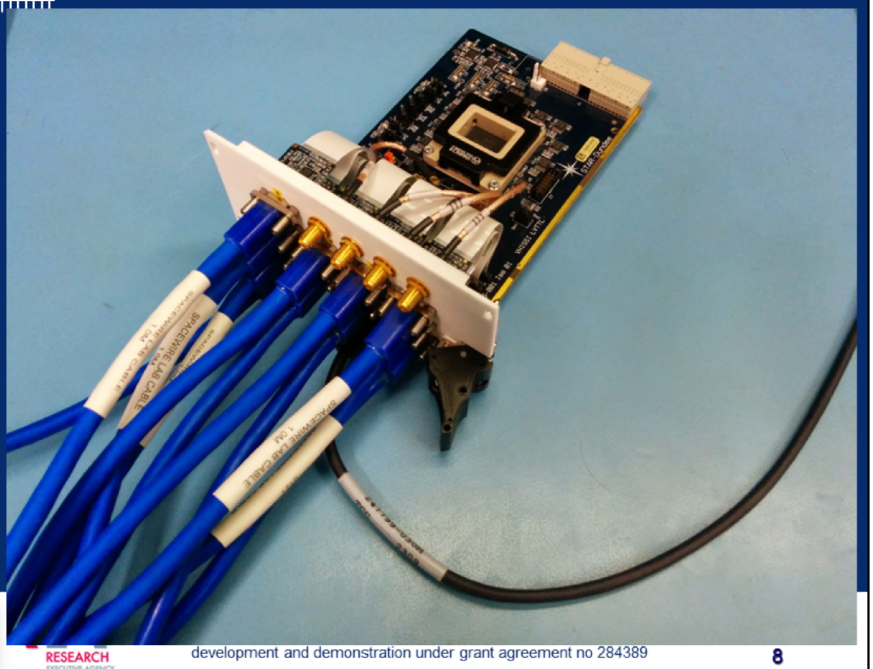
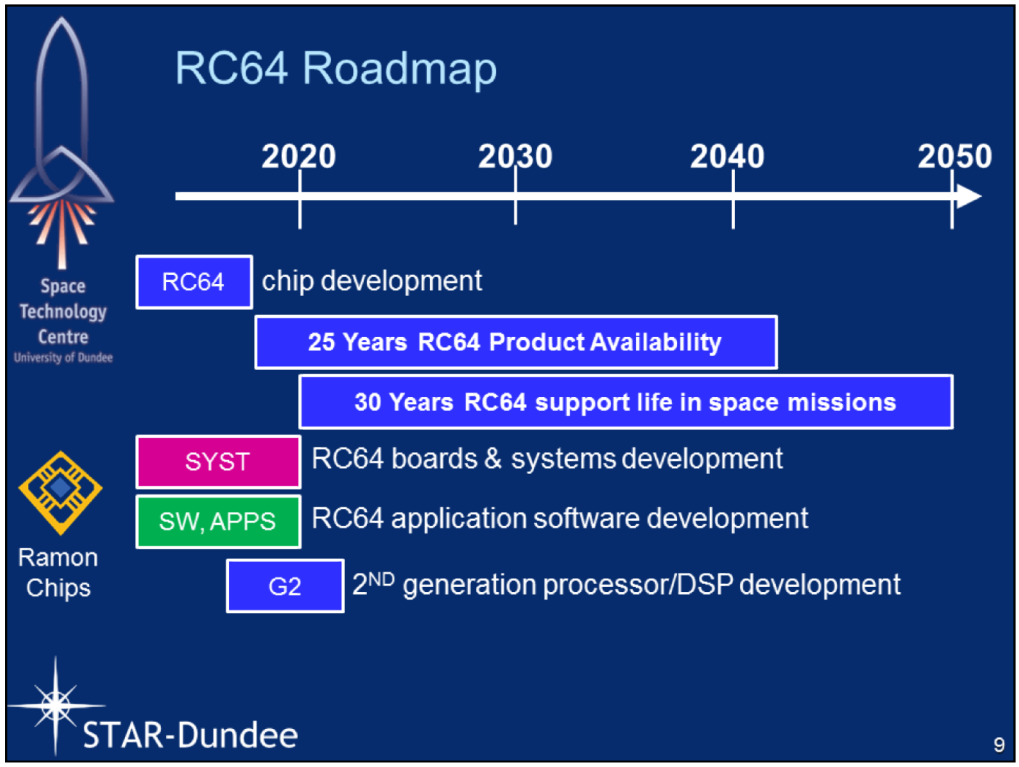
VHiSSI

SpaceWire Concentration



RESEARCH EXECUTIVE AGENCY

development and demonstration under grant agreement no 284389


RC64 Roadmap
2020
2030
2040
2050
Space Technology Centre
University of Dundee
RC64
chip development
25 Years RC64 Product Availability
30 Years RC64 support life in space missions
SYST
RC64 boards & systems development
SW, APPS
RC64 application software development
Ramon Chips
G2
2ND generation processor/DSP development
STAR-Dundee
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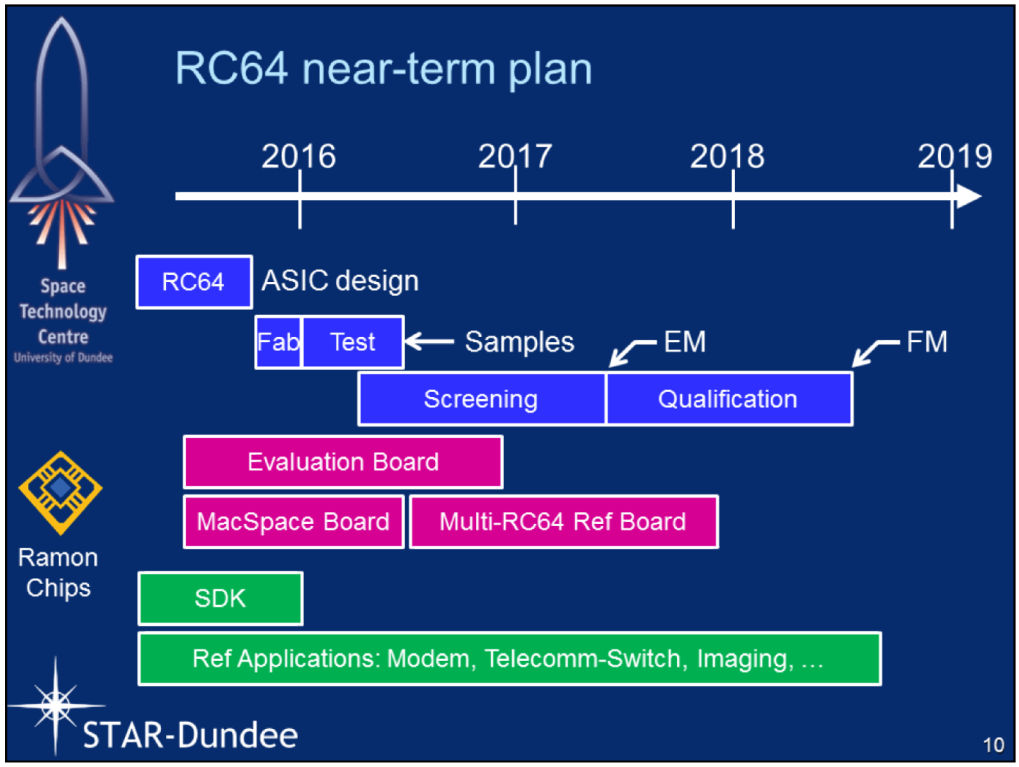
RC64 near-term plan
2016
2017
2018
2019
Space Technology Centre
University of Dundee
RC64
ASIC design
Fab
Test
Samples
EM
FM
Screening
Qualification
Evaluation Board
MacSpace Board
Multi-RC64 Ref Board
Ramon Chips
SDK
Ref Applications: Modem, Telecomm-Switch, Imaging, …
STAR-Dundee
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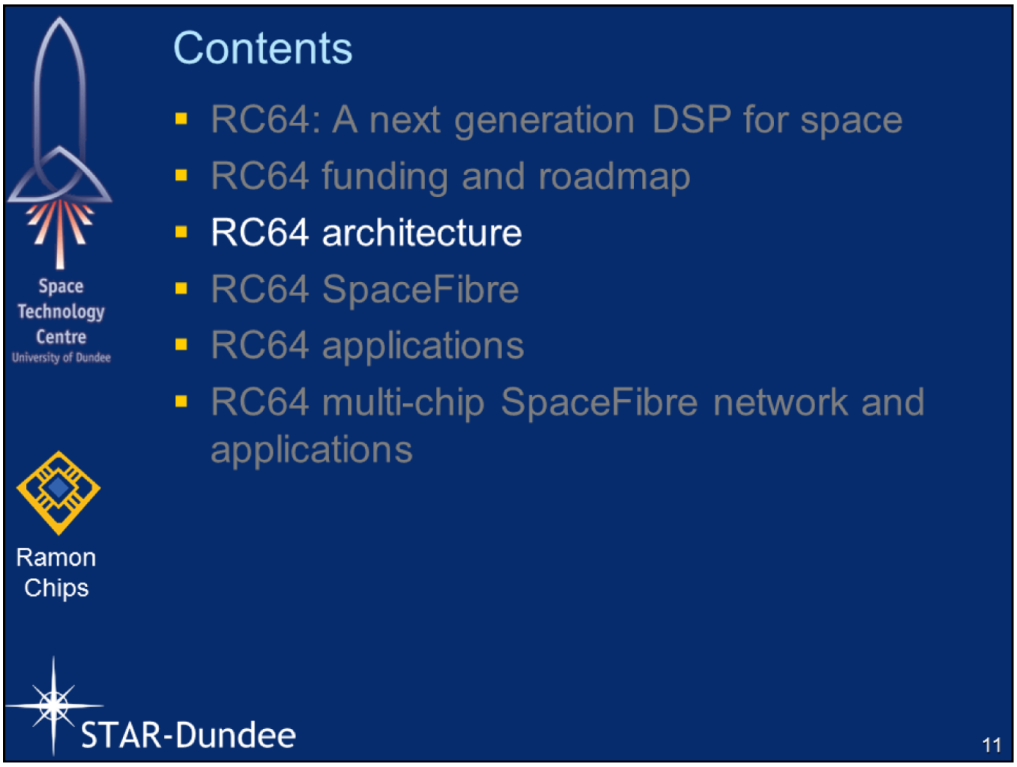
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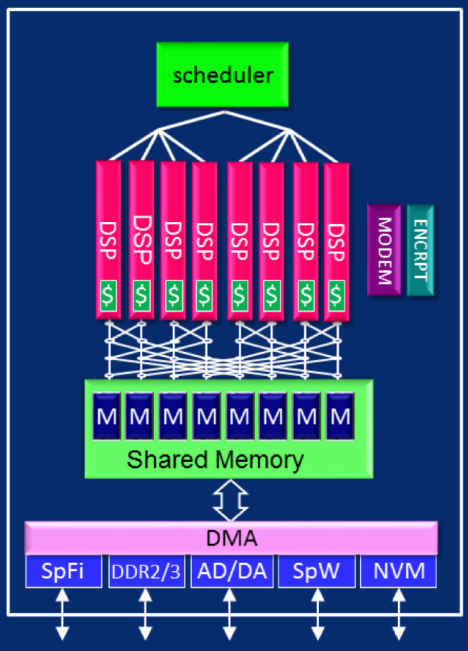
RC64

- 64 fast CEVA X1643 DSP with FP extension and HW scheduler
  - 300 MHz
  - 40 GFLOPS, 384 GOPS
- Modem and Encrypt accelerators
- 4 Mbyte on-chip shared memory
- Fast I/O
  - SpFi, DDR3, AD/DA LVDS I/F, SpW, NVM
- Rad-Hard, for space
- Advanced technology
  - TSMC 65nm LP
  - CCGA / PBGA / COB
  - 10 Watt
- Modular
  - Payloads can employ many RC64
- Versatile
  - Designed for all space missions
  - Planned for 2020—2050
- Re-programmable in space
- Compatible with ESA and NASA roadmaps



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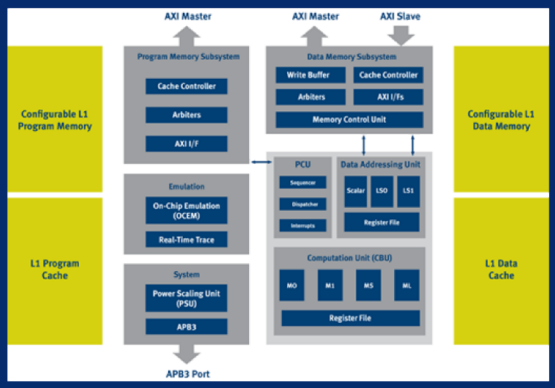
CEVA X1643 DSP core



- VLIW+SIMD
  - L/S, L/S, MAC, MAC, MAC, MAC, addr, bit-manipulation, …
  - Two caches and “scratch pad” memory
  - Floating point fused multiply-add (MAC)
- High performance, low power, ITAR-free, software-rich core
- CEVA joined as partner in FP7 MacSpace project to ensure suitability for space

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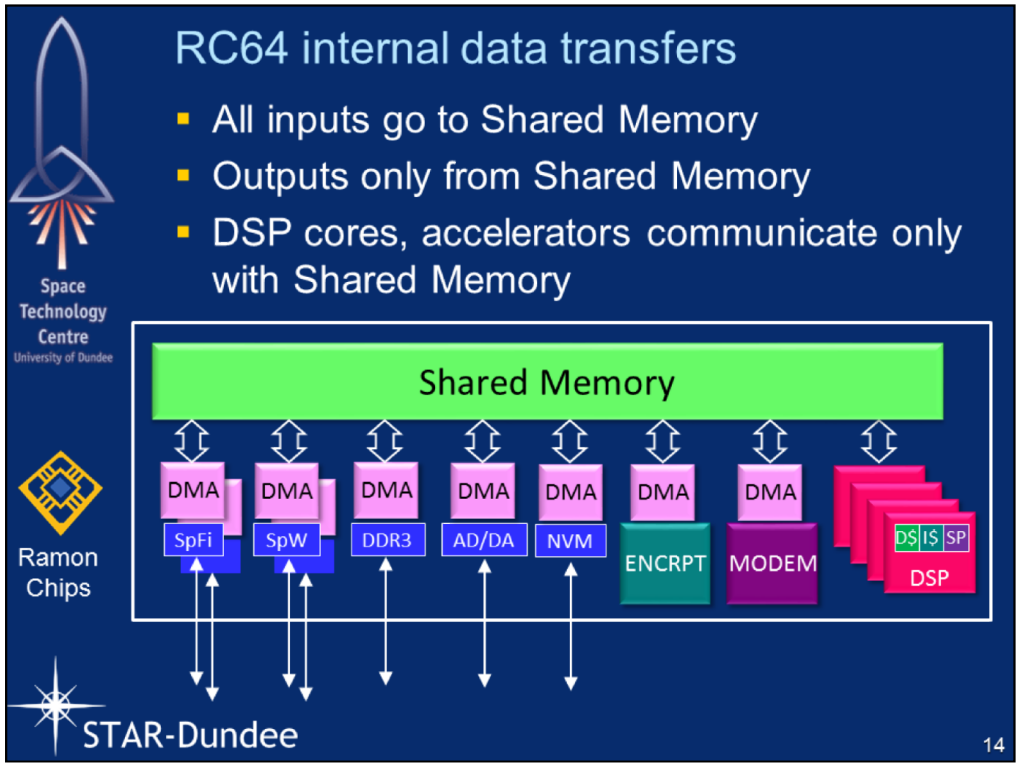
RC64 internal data transfers
All inputs go to Shared Memory
Outputs only from Shared Memory
DSP cores, accelerators communicate only with Shared Memory
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University of Dundee
Ramon Chips
Shared Memory
DMA
SpFi
SpW
DDR3
AD/DA
NVM
ENCRPT
MODEM
DS
IS
SP
DSP
STAR-Dundee
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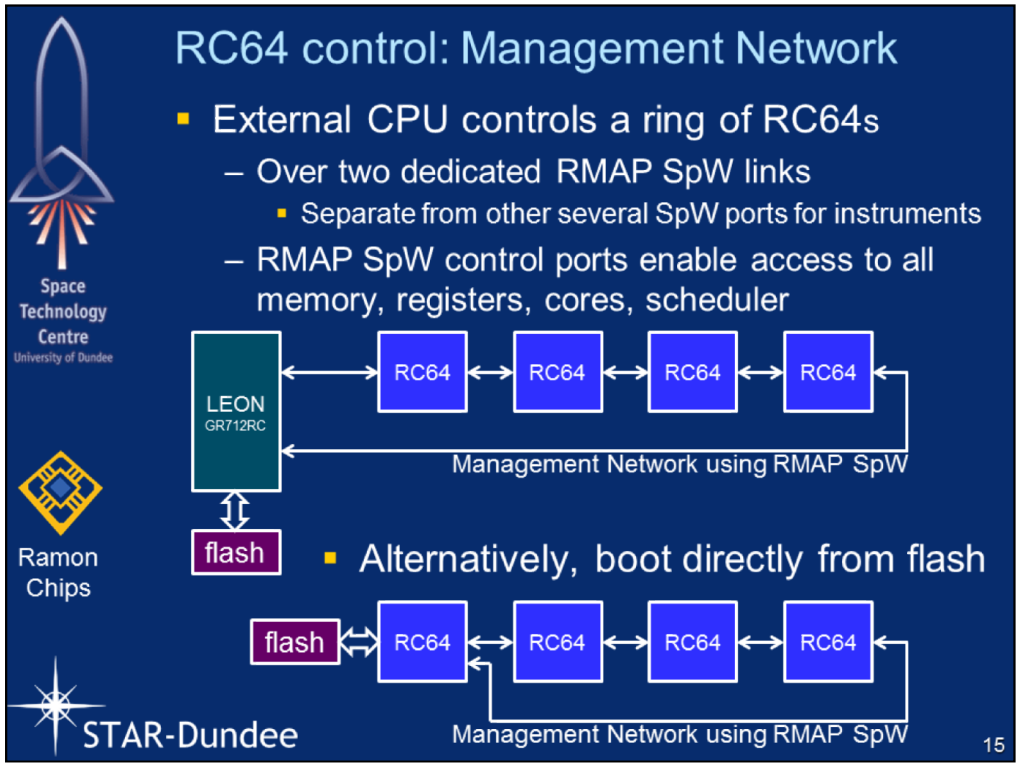
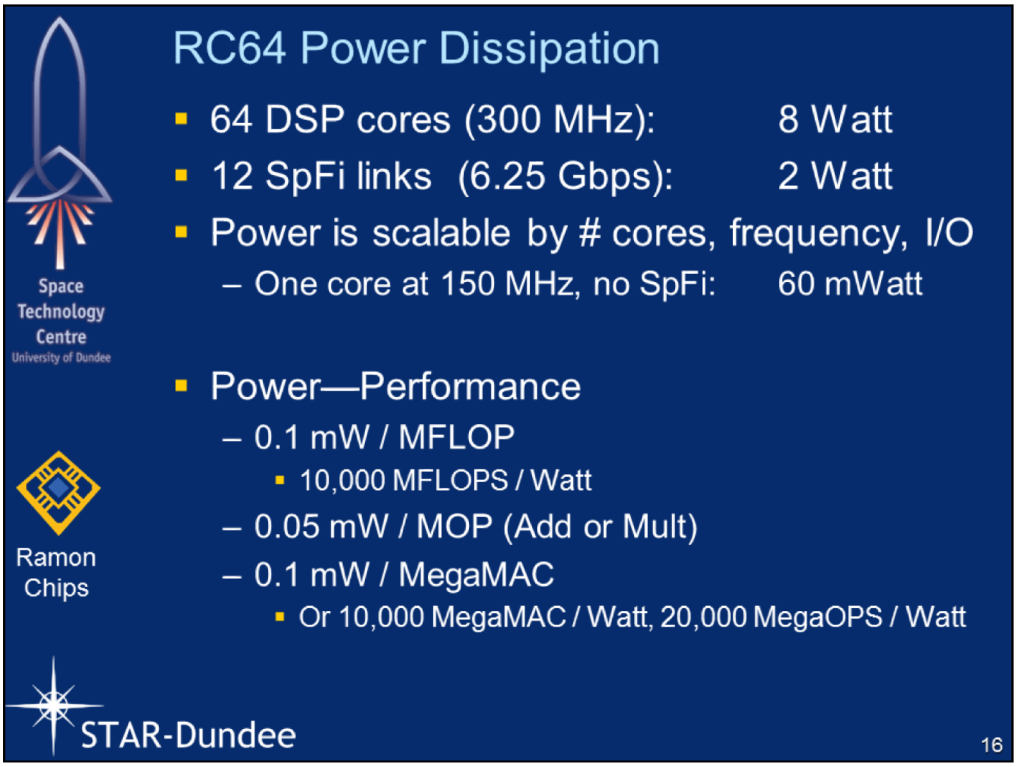


The host processor (LEON GR712RC in the slide) is in charge of boot, code distribution to the RC64 chips, monitoring their activity, collecting data on radiation events, recovery in case of faults, and security.


RC64 Power Dissipation
64 DSP cores (300 MHz): 8 Watt
12 SpFi links (6.25 Gbps): 2 Watt
Power is scalable by # cores, frequency, I/O
One core at 150 MHz, no SpFi: 60 mWatt
Power—Performance
0.1 mW / MFLOP
10,000 MFLOPS / Watt
0.05 mW / MOP (Add or Mult)
0.1 mW / MegaMAC
Or 10,000 MegaMAC / Watt, 20,000 MegaOPS / Watt
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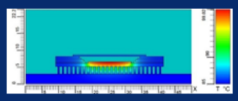
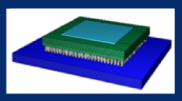
RC64 Package Options

- Thermal cycling control by HW & SW
  - Temp sensors on-chip, SW maintains fixed temp
  - Mitigation of column / ball shearing due to cycles

1. CCGA 624
   - Wire bonded





2. PBGA 624
   - Wire bonded
3. Optional FC-PBGA 624
   - Flip-chip, top-level heat removal
4. Optional Chip-on-Board
   - Bare die flip-chip assembly in MCM-SiP

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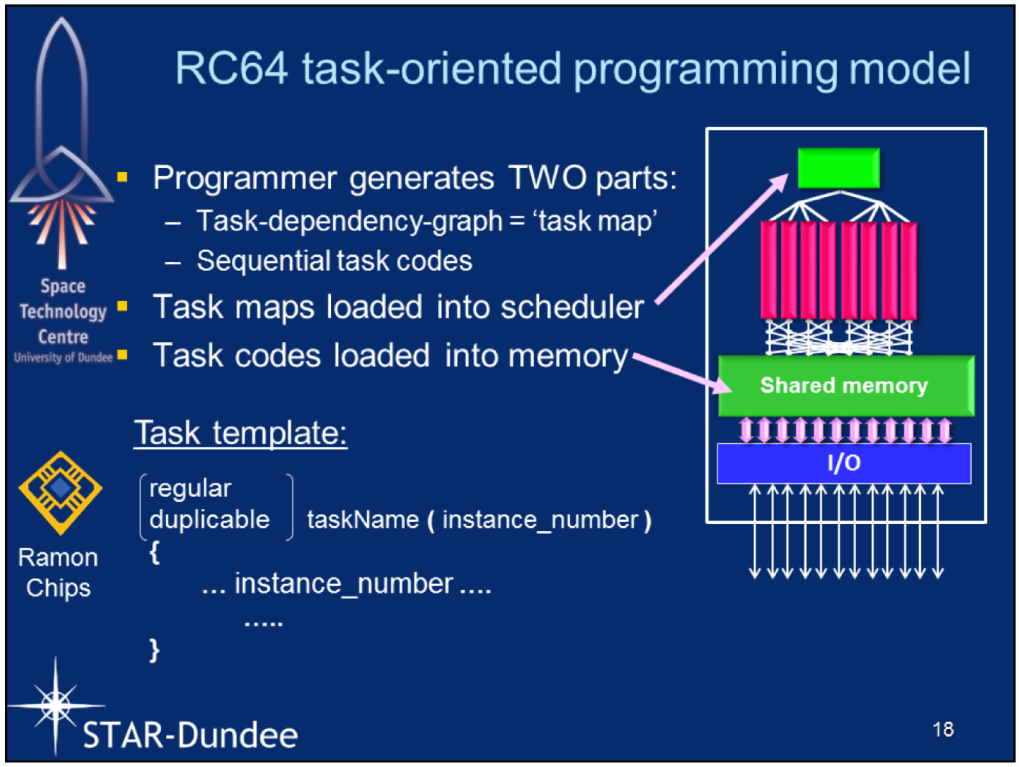


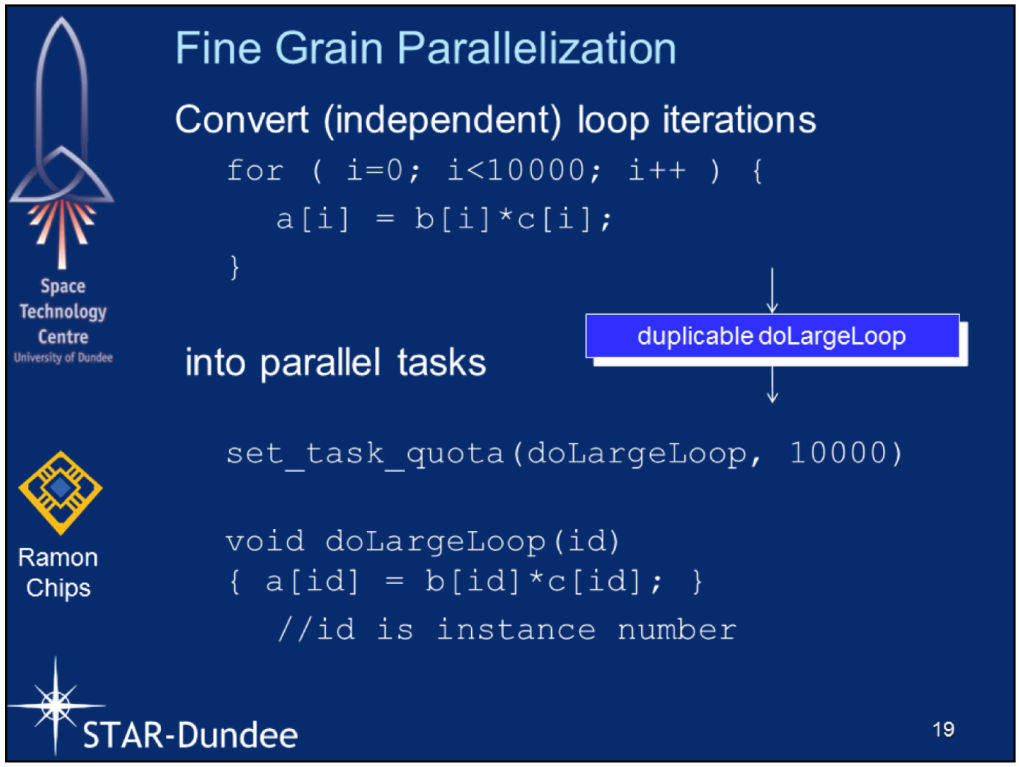
Duplicable tasks are designed for data parallelism: Written once, executed in many copies (instances)

Each instance receives a unique number (when dispatched by the scheduler). The instance number enables the task code in accessing its unique data in shared memory.

Each core can execute any task and any instance.

The scheduler dispatches a task (or instance) by sending TWO numbers to a core: code entry point, and instance number.

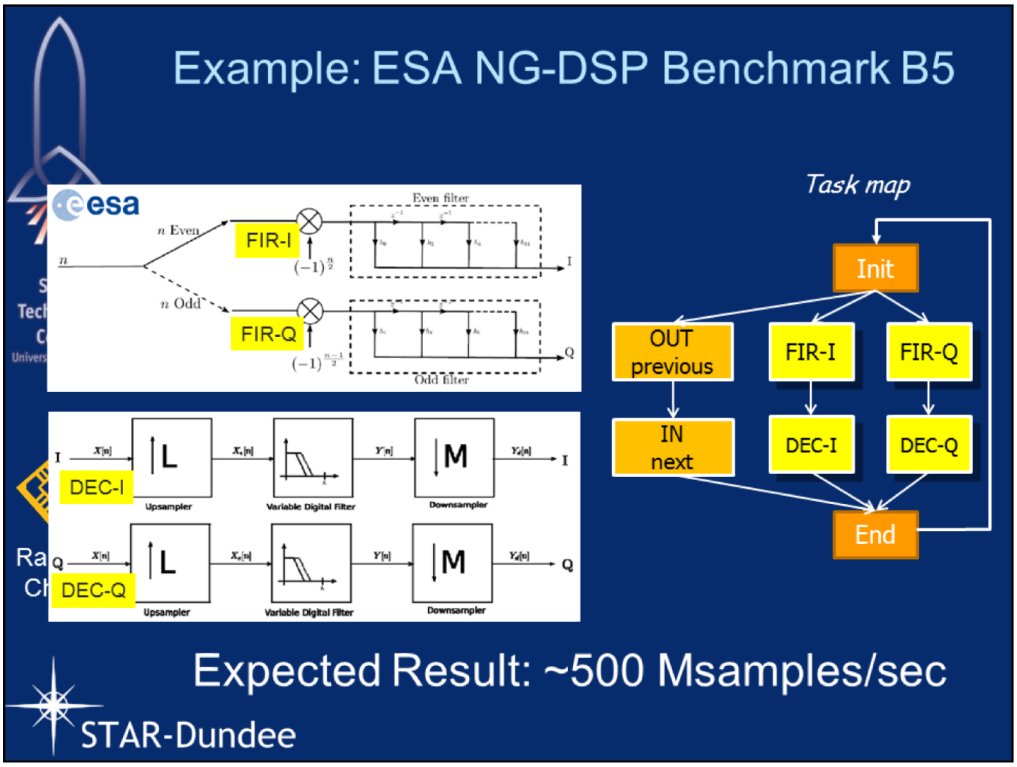
When the core completes execution, it sends a token back to the scheduler.



Task map is a single box in this case (shadow means duplicable task)

Each instance computes ONE data element.

Number of instances equals number of data elements. Rather than equal to the number of cores !



ESA created several benchmarks for DSP

B5 is communication (diagram on left is from ESA doc): Demodulation (left top) followed by decimation filter (left bottom).

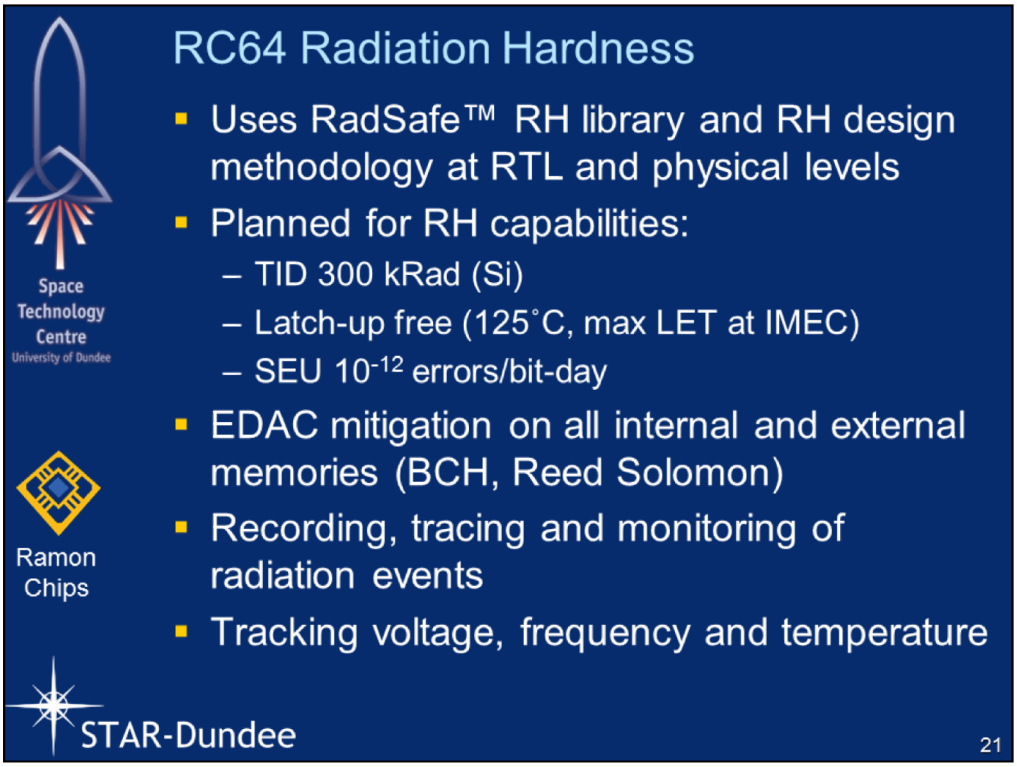
Streaming of infinite input.

On the right, we show TASK MAP for this on RC64.

Each iteration is applied to one large data block (we used 8k samples per block)

Input of next block and output of the results of previous block take place in parallel with processing present block.

Result: cf. 7 Msamples/sec on ESA-21469 [John Frank, Astrium-UK, presentation at ESA DSP Day 2012].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Ramon Chips
STAR-Dundee
RC64 Radiation Hardness
Uses RadSafe™ RH library and RH design methodology at RTL and physical levels
Planned for RH capabilities:
– TID 300 kRad (Si)
– Latch-up free (125˚C, max LET at IMEC)
– SEU 10-12 errors/bit-day
EDAC mitigation on all internal and external memories (BCH, Reed Solomon)
Recording, tracing and monitoring of radiation events
Tracking voltage, frequency and temperature
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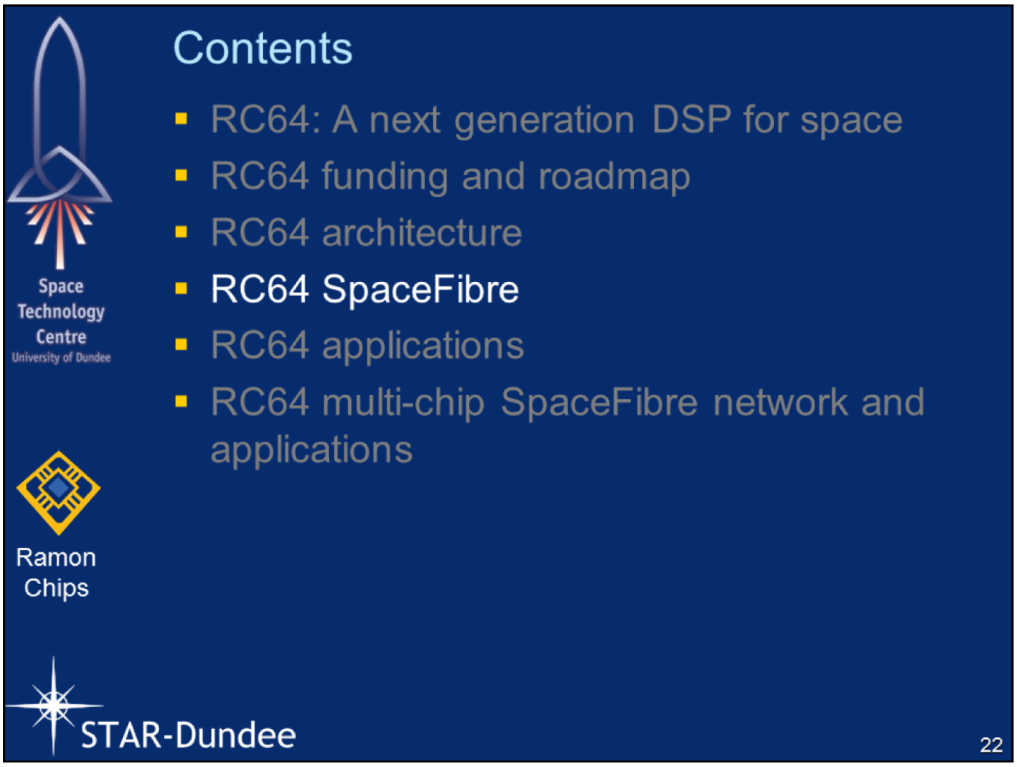
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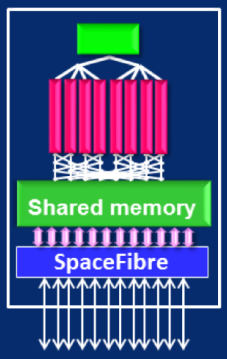
RC64 SpaceFibre



- 12 ports
  - 2.5 / 3.125 Gbps on slow package
  - 5.0 / 6.25 Gbps on fast package
  - Total 30 or 60 Gbps bandwidth
- Ports implement
  - Physical Layer
  - Link Layer
  - Quality Layer
- Each port interfaced to own DMA controller
  - All traffic to/from Shared Memory on-chip
- Software on RC64 cores implements (as needed)
  - Multi-Lane Layer
  - Network Layer

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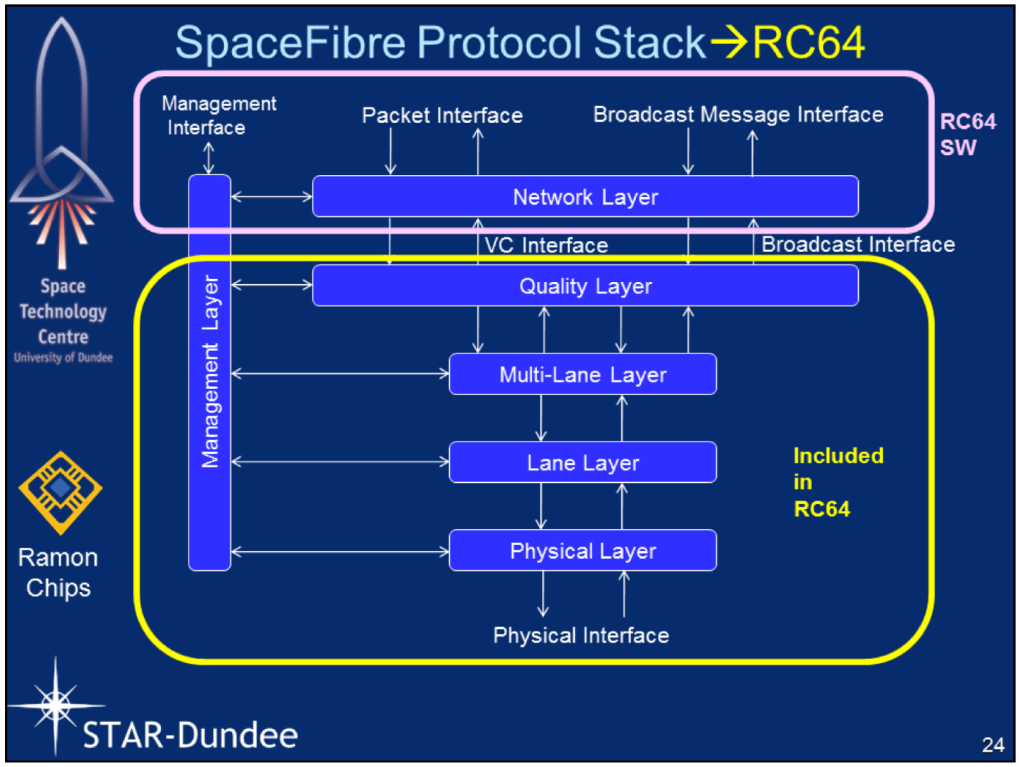
SpaceFibre Protocol Stack→RC64
Management Interface
Packet Interface
Broadcast Message Interface
RC64 SW
Network Layer
VC Interface
Broadcast Interface
Management Layer
Quality Layer
Multi-Lane Layer
Lane Layer
Physical Layer
Included in RC64
Physical Interface
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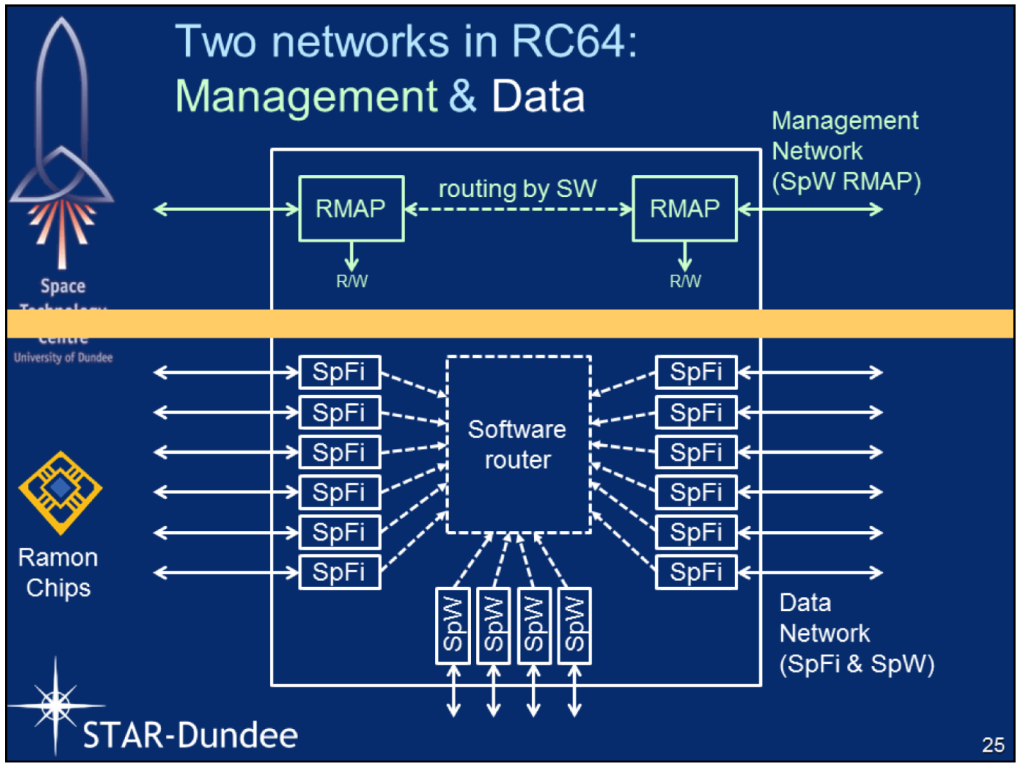
Two networks in RC64:
Management & Data
Management
Network
(SpW RMAP)
RMAP
routing by SW
RMAP
R/W
R/W
Space
University of Dundee
SpFi
SpFi
SpFi
SpFi
SpFi
SpFi
Software
router
SpFi
SpFi
SpFi
SpFi
SpFi
SpFi
SpW
SpW
SpW
SpW
Ramon
Chips
Data
Network
(SpFi & SpW)
STAR-Dundee
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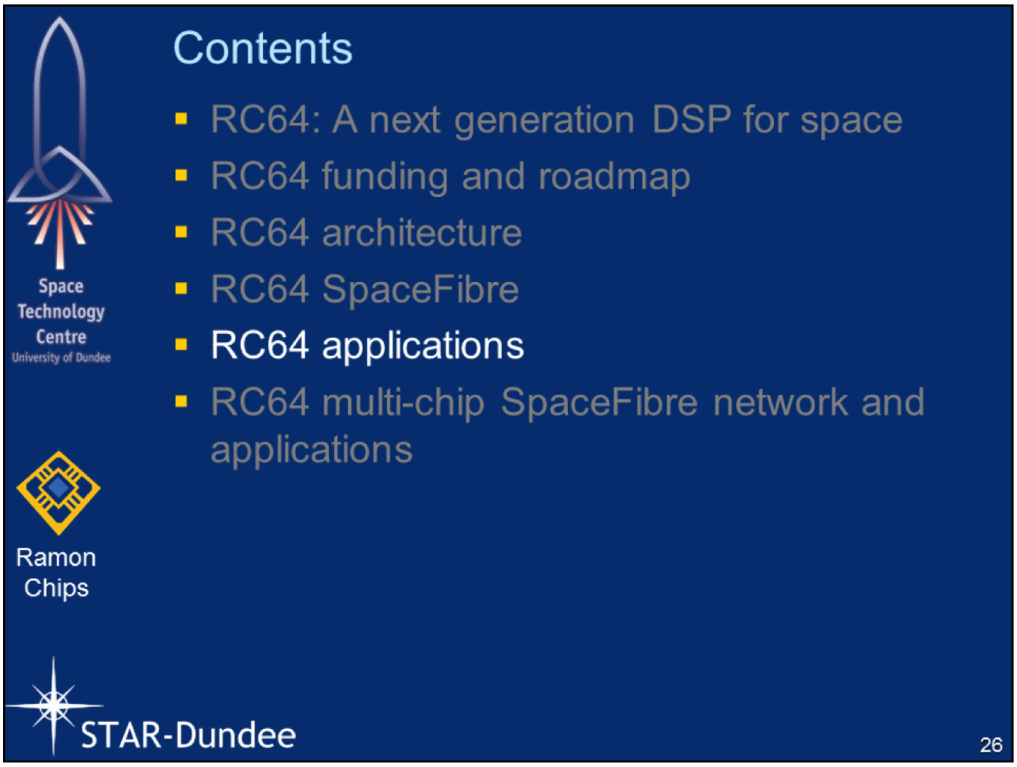
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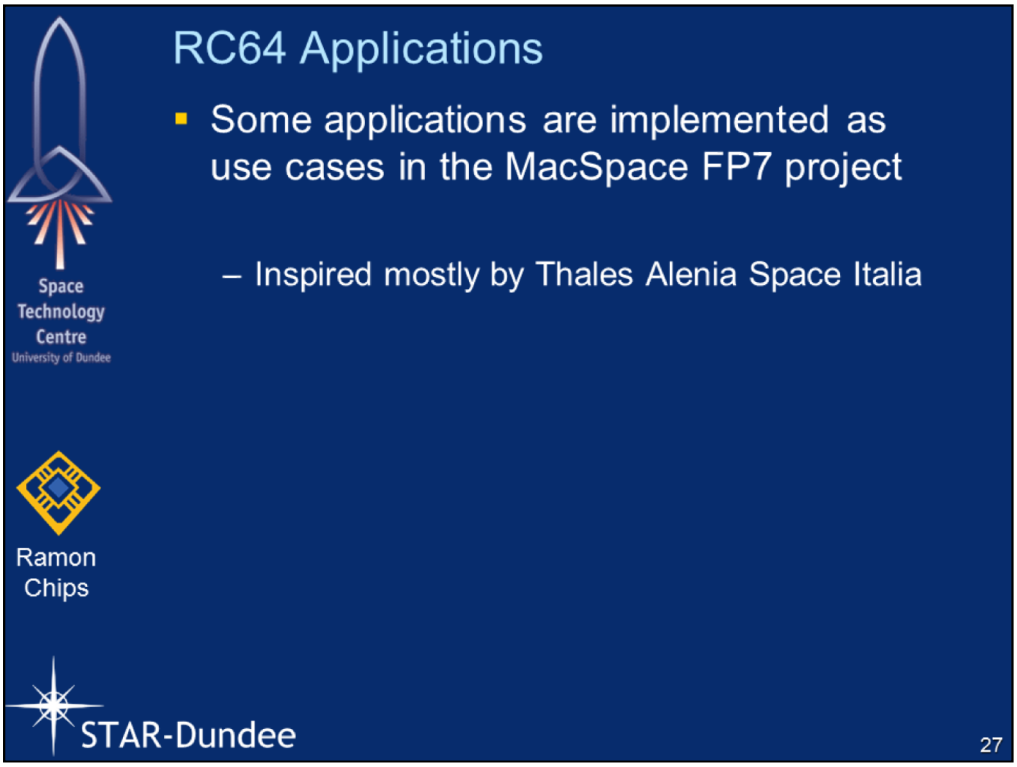
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RC64 Applications
Some applications are implemented as use cases in the MacSpace FP7 project
– Inspired mostly by Thales Alenia Space Italia
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Needs for supercomputing in space

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Image understanding and prompt utilization, e.g., disasters

OUTER SPACE
Autonomous smart robots

Smart switching, high bandwidth and capacity, space internet, global mobile communications

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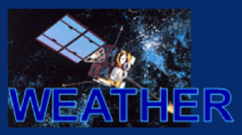

Time, place accuracy of prediction

In-space location computation of space, air, marine and land objects

RADAR

Imaging and locations at night and all weather

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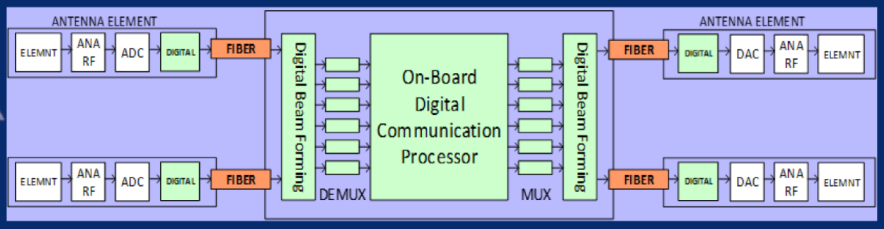
Telecomm Digital Payload



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- Advanced telecom satellite
  - Phased array antenna with digital elements
  - Massive antenna-to-body interconnect
  - On-board processor:
    - Digital beam forming
    - Frequency multiplexers
    - Transparent switching (FDM / TDM)
    - IP routing (with modems)
    - Higher levels processing

Each green box means RC64

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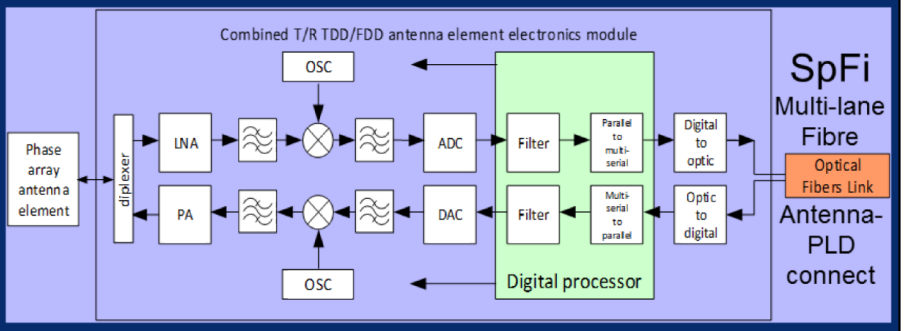
Phased Array Antenna digital module

In antennas with
100s—1000s of modules



- Digital tasks in the antenna element
  - Sampling rate reduction (gain more bits)
  - Multi-lane HSSL for antenna-to-body interconnect

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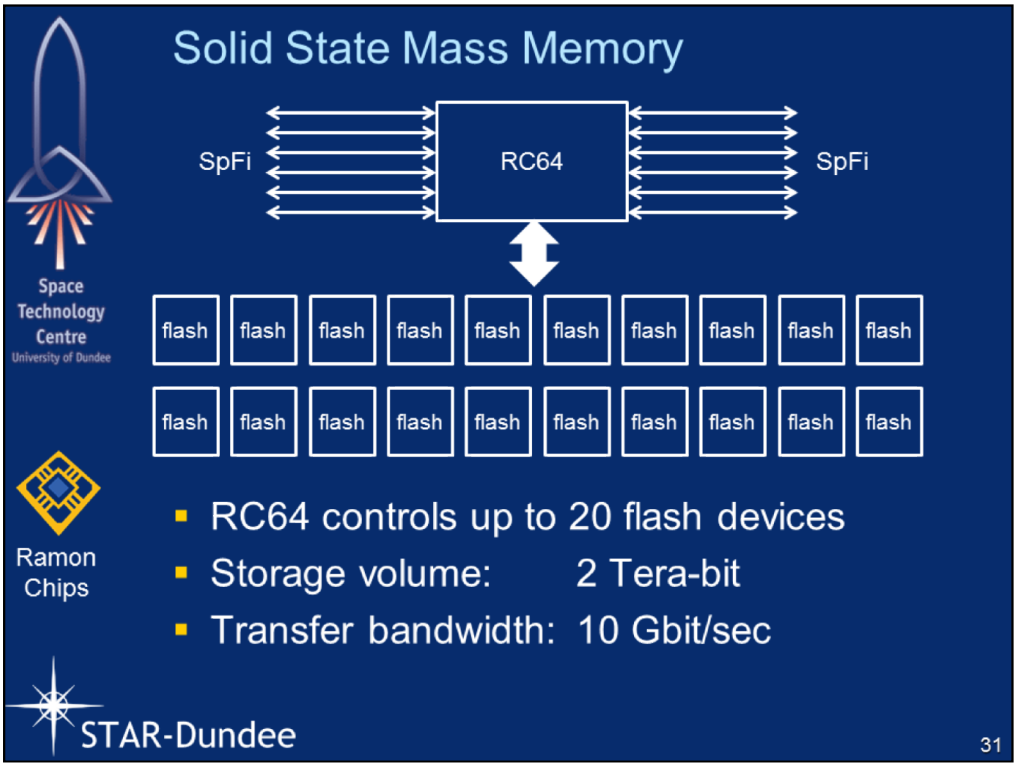
Solid State Mass Memory
SpFi
RC64
SpFi
flash
Space Technology Centre
University of Dundee
Ramon Chips
RC64 controls up to 20 flash devices
Storage volume: 2 Tera-bit
Transfer bandwidth: 10 Gbit/sec
STAR-Dundee
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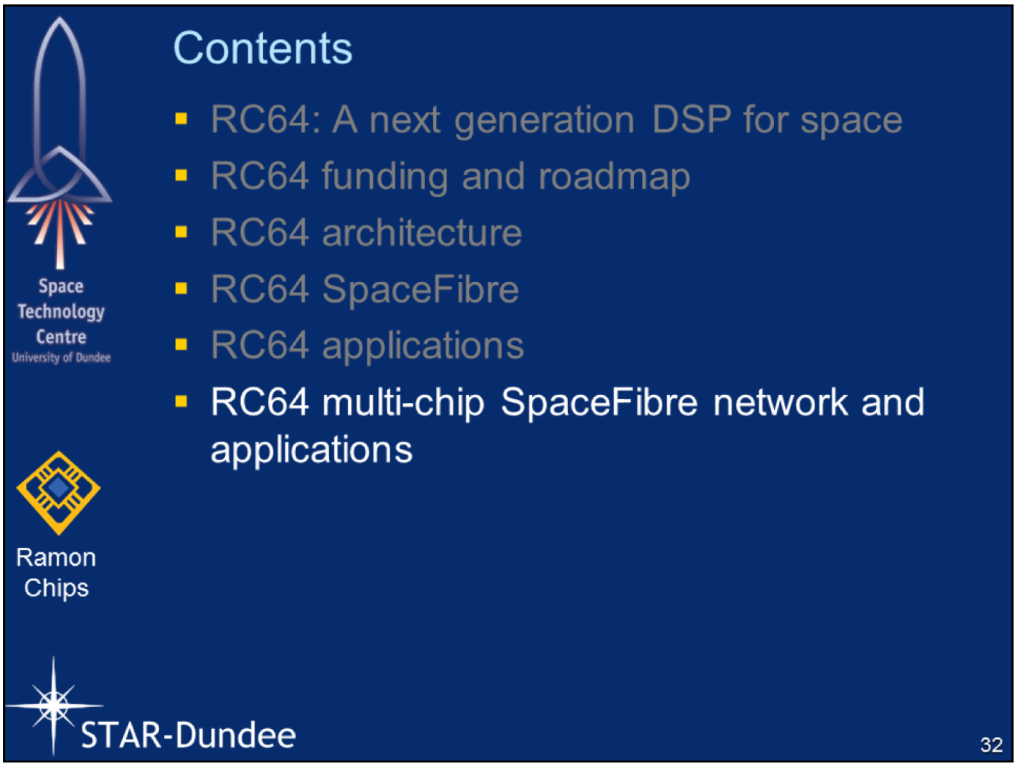
Space
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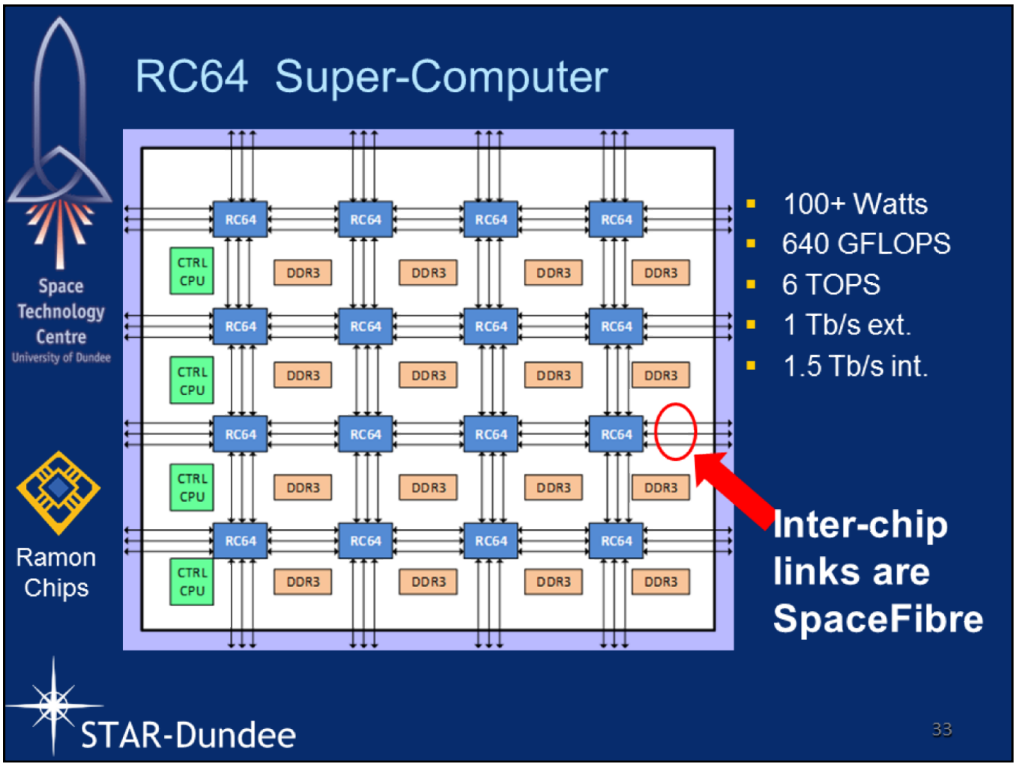
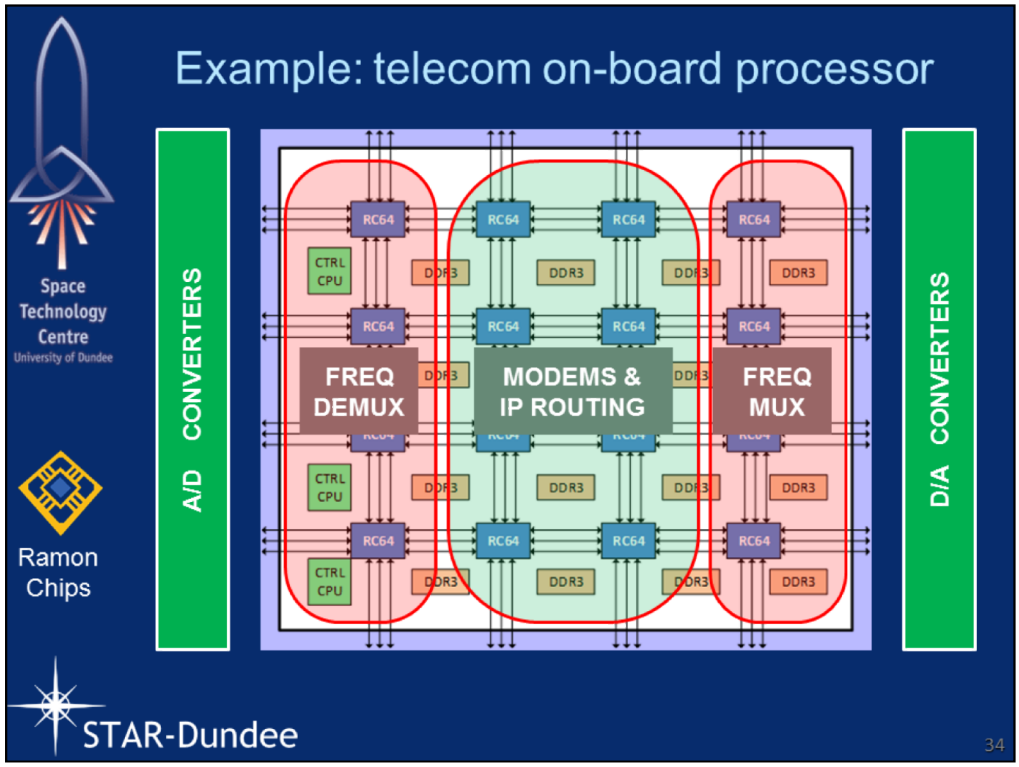
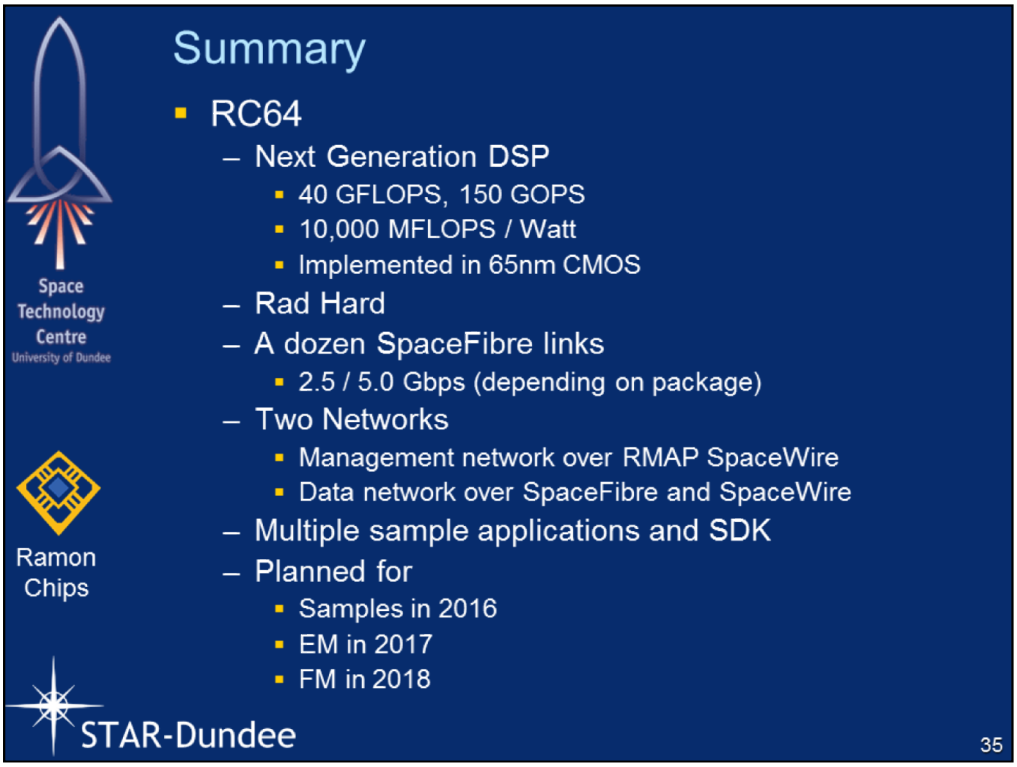


Each RC64 may be equipped with:

- Own DDR3 memory
- Own NVM (Flash) memory (not shown)
- SpaceWire links to instruments (not shown)
- Interface to ADC and / or DAC (not shown)
- POL voltage regulators



Mapping of applications to groups of RC64 ASICs is flexible, manageable by the control (host) processors, reconfigurable while in orbit



Summary

- RC64
  - Next Generation DSP
    - 40 GFLOPS, 150 GOPS
    - 10,000 MFLOPS / Watt
    - Implemented in 65nm CMOS
  - Rad Hard
  - A dozen SpaceFibre links
    - 2.5 / 5.0 Gbps (depending on package)
  - Two Networks
    - Management network over RMAP SpaceWire
    - Data network over SpaceFibre and SpaceWire
  - Multiple sample applications and SDK
  - Planned for
    - Samples in 2016
    - EM in 2017
    - FM in 2018