A Design Flow for FPGA Conversion into Radiation-Hardened ASIC

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Abstract

The technology and design flow used for converting FPGA designs into two rad-hard ASICs is described. The ASICs are JPIC, an image compression ASIC using JPEG2000 standard, and GR712RC, a dual core LEON3FT processor. Both ASICs employ the Rad-Hard-By-Design RadSafe™ technology, and are implemented on a standard 180nm CMOS technology. Each ASIC is 12×12mm, integrating more than 40 million transistors. RadSafe™ technology provides very high immunity to all radiation effects. The library was designed for high immunity to radiation and high reliability. It includes standard logic cells, SRAMs, all-digital DLL and I/O cells. It was proven on several test chips, demonstrating TID immunity in excess of 300Krad, SEL immunity above 80MeV and SEU at 20μ^2 cross section (10^{-12} errors/bit/day). Logic design includes EDAC, memory BIST, and techniques to minimize soft errors. Logic synthesis was performed with large timing margins and scan insertion. Physical synthesis includes a robust power grid, careful placement of I/O cells, immunity to process sensitivities, robustness to thermomechanical stress and packaging reliability. A custom 240 pins CQFP ceramic package for GR712RC was optimized for mechanical stress, hermeticity, improved supply connection for reduced impedance, and robustness to handling. A custom 208 pins PQFP plastic package was designed for JPIC. Both designs were first implemented on high-end FPGAs and subsequently converted to ASICs.

EXTENDED ABSTRACT

Introduction

Space products should provide very high reliability and immunity to all radiation effects. The immunity should be guaranteed prior to finalizing the product. It typically requires the use of Radiation Hardening By Design (RHBD) [1,2], Design For Reliability (DFR), Design For Testability (DFT) and development of hi-rel custom packages. The RHBD concept enables fabricating the devices on a low cost, mature and reliable CMOS process. It simplifies export restrictions, making RHBD preferred over radiation hardening by process. It enables replacing radiation-sensitive FPGAs into ASICs.

Commercial libraries and hard IP cores, which are not designed for space, do not guarantee sufficient immunity to radiation effects. Thus, immunity of Custom off-the-Shelf (COTS) parts can be checked only after production. RadSafe™ technology, which is optimized for space and high reliability applications, guarantees the required immunity to all radiation effects.

SRAM cores are typically the most sensitive circuits. Their dense geometry increases the susceptibility to Total Ionizing Dose (TID), Single Event Latch-up (SEL) and Single Event Upsets (SEU). We developed embedded SRAM cores that eliminate the key mechanisms of TID and SEL failures. SEU immunity is enhanced by Error Detection and Correction (EDAC) logic. The integrity of the SRAMs is tested by dedicated built-in self-test (BIST) that enables read and write access to all bits from external pins.

High speed applications often require PLL or DLL for frequency multiplication and clock de-skewing. Analog PLL/DLL cores are very sensitive to strikes of ionized particles, which might cause very large jitter and undesired spikes. The use of all-digital DLL eliminates the issues that exist in the analog cores.

I/O buffers require special attention, due to higher sensitivity to latch-up in ESD protection circuits, and due to thermomechanical stress when using plastic packages. The high inductance packages require special techniques for reduction of voltage drops during Simultaneous Switching Outputs (SSO). Bonding pads and bond wires should be highly immune to various mechanical stresses.

The requirement for high quality and reliability requires high testability by using high functional coverage in test, based on scan, memory BIST, NAND tree and Iddq testing.

The following sections describe key concepts of the design flow that assure the high immunity to space environment.

The RadSafe™ cell libraries

The ASIC building blocks that provide the immunity to TID and SEL are the basic cells. RadSafe™ libraries are designed specifically for this purpose. They include the following four libraries.

The *Standard logic cell library* is designed to provide high immunity to TID and SEL, independent of placement. The SEU/SET effects are mitigated by proprietary soft-error protected flip flops, which provide better immunity than TMR with much lower area and power. The cells have been characterized, and are used in the synthesizable design flow.

The *I/O cell library* provides high immunity to TID and SEL, high immunity to SSO and ground bouncing, special rad-hard ESD protection and high immunity to thermomechanical stress. Large pads are included for bonding with thick bond wires, meeting Class S requirements.

The *SRAM library* includes single and dual port memories that utilize special circuit techniques for mitigation of TID and SEL effects. The mitigation of SEU is mostly achieved by synthesized EDAC, integrated into the SRAM macro cell. Controllability and observability for testing are achieved by integrating BIST logic into the macro cell. The cores are configurable to any size, up to 2048 words address space and 40 bits of data. Larger arrays are constructed by combining multiple SRAM blocks using synthesized logic.

The *DLL library* offers several all-digital rad-hard DLL cores, using RadSafe™ standard cells. It enables frequency multiplication by 2X or 4X, clock de-skewing and splitting the cycle into multiple phases. These cores consume low active power, negligible standby power and small area, and produce very low jitter.

We developed the RadSafe™ standard cell library in two versions: 1.8V version for optimized power and performance, and 3.3V for compatibility enabling direct "drop-in" replacement of existing FPGAs. Both libraries were tested for all radiation effects, and showed similar immunity.

The use of RadSafe™ libraries is complemented by methodology for optimizing the RHBD flow and achieving high reliability.

Automatic design flow

Both ASICs were designed at the logic level mostly by third party IP vendors that provided proven IPs. The vendors updated the logic to comply with RadSafe™ methodology requirements and cell libraries. The final VHDL code, including complementary logic designed by Ramon Chips, was validated by intensive simulations, synthesizing it to FPGA, and checking it at full speed in the target system environments.

Logic synthesis was performed with a standard synthesizer, combining also a variety of standard small IP cores. Physical design was carried out with a typical back-end suite, including floor planning, clock tree synthesis, automatic timing verification and correction, scan chain re-ordering. A proprietary macro created a robust custom power grid. The post layout verifications required an extraction tool, a static timing verification tool, and signal integrity checking tools. Final layout verifications were done by DRC and LVS checkers, and were re-checked by the foundry.

Test patterns for scan checks were generated by an ATPG tool. The test vectors for memory checks were developed by using the MARCH-C algorithm [3], and activating the embedded memory BIST. Functional test vectors were generated by the functional simulator at the logic level.

Examples of ASICs

The two ASICs, GR712RC and JPIC, have been designed for the same die size, and are processed on the same wafer. Wafer sharing is economical in light of the small unit counts that are typically required for space applications. Having both dies the same size simplifies the sawing process during assembly. Each die size is 12×12mm. The ASICs are processed with 0.18µm CMOS technology by Tower Semiconductors, with 6 metal layers.

Microphotographs of the two ASICs are shown in Figure 1. JPIC integrates about 250 SRAM cores, 2 DLLs, 208 I/O pins, and about 1.1M gates. It operates at 88MHz, and consumes less than 3W. GR712RC integrates about 100 SRAM cores, mostly for the cache and the on-chip scratchpad memory block, 2 DLLs, 240 I/O pins and about 0.6M gates. It operates at frequencies above 100MHz and consumes about 2W.

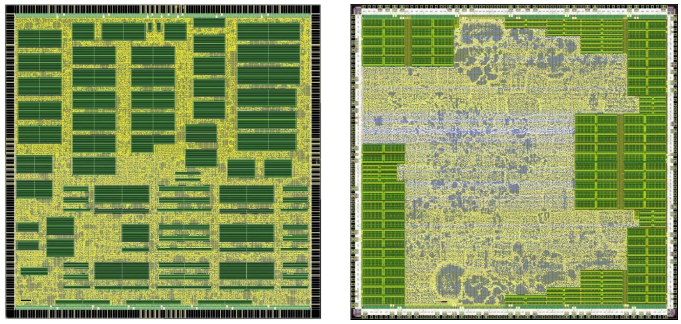

Figure 1: Die photo of JPIC (left) and GR712RC (right)
(the drawings will be replaced by photos once the chips are available)

Package development

GR712RC supports many I/O ports, calling for a high pin count package. We opted for CQFP, which is more reliable and less costly for all space applications than alternative CCGA packages. We chose 240 pins CQFP package thanks to its small physical size, a key consideration in high speed ASICs. However, since 240 pins are insufficient for all the I/O requirements of GR712RC, we introduced programmable I/O configurations, where only a subset of the interfaces is available on I/O pins in each configuration.

The package is custom designed. It has an isolated tie bar, protecting the leads during handling and testing. The multilayer package provides dedicated layers for GND, VDD and VDDIO, minimizing inductance on these supply pins. All bond wires are short, parallel, with large inter-wire spacing, for immunity to shock, vibration and thermal cycling. The bonding pads on the die are very large, enabling the use of thick aluminum wires. All these features enable Class S quality level. Figure 2 presents the package of GR712RC.

The JPIC is packaged in PQFP 208L, custom designed for this chip. It uses an exposed heat spreader that should be attached to a thermal pad on the PCB.

Testing and qualification

The GR712RC will be qualified as a Class-S product. In addition to the standard requirements specified in the standard, it will be screened by a proprietary test methodology for detection of many degradation mechanisms during the tests, to enable the elimination of weak parts before shipment.

Summary

Two advanced ASICs were converted from FPGAs by Ramon Chips and partners for space applications. They use RadSafe™ libraries and a design flow that are optimized for these applications. High reliability is assisted by a special package development and by custom screening procedure.

References

[1] R.C. Lacoe et al, "Application of Hardness-By-Design Methodology to Radiation-Tolerant ASIC Technologies", IEEE Transactions on Nuclear Science, Vol. 47, No. 6, Dec. 2000, pp. 2334-2341.

[2] R.C. Lacoe et al, "Total-Dose Tolerance of the Commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-µm CMOS Process", IEEE Transactions on Nuclear Science, Dec. 2001, pp. 72-76.

[3] M.L Bushnell & V.D. Agrawal, Essentials of Electronic Testing for Digital & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, pp. 281-296.