JPIC - Rad-Hard JPEG2000 Image Compression ASIC

Ran Ginosar and Dov Alon, Ramon Chips Ltd., Israel
Nikos Zervas, Alma Technologies S.A., Greece
Amitai Broyde, MBT Ltd., Israel

ABSTRACT

JPIC is a rad-hard high-performance image compression ASIC for space applications. It implements tier 1 of the ISO/IEC 15444-1 JPEG2000 (a.k.a. J2K) image compression standard [1] as well as the post compression rate-distortion algorithm, which is part of tier 2 coding. A modular architecture enables employing a single JPIC or multiple coordinated JPIC units. JPIC is designed to support any size of imager in optical, panchromatic and multi-spectral space and airborne sensors. A similar implementation on a high-end FPGA device is described. It has been employed for verification and validation. JPIC has been developed as a collaboration of Alma Technologies S.A. (Greece), MBT/IAI Ltd (Israel) and Ramon Chips Ltd (Israel). The JPEG2K-E IP core from Alma implements the compression algorithm [2]. The IP core has been designed for both FPGA and ASIC implementations. Ramon Chips has added SERDES and host interfaces and has integrated the ASIC. MBT has validated the full chip on an Altera Startix-III FPGA and created system boards employing multiple JPIC ASICs. The ASIC implementation, based on Ramon Chips' 180nm CMOS RadSafe[TM] RH cell library enables superior radiation hardness. The ASIC is fabricated on Tower Semiconductor process. The ASIC is packaged in either plastic QFP 208 or a similar ceramic package.

EXTENDED ABSTRACT

Introduction

An image compression solution has been sought for a series of imaging satellites to be developed in Israel. For purposes of quality and compatibility, the JPEG2000 standard has been selected. Available commercial chips failed in radiation tests and were determined unqualified for both short- and long-term space missions. Hence, two custom solutions were considered: FPGA and ASIC implementations. The FPGA implementation was also found unqualified for use in space. A rad-hard ASIC was developed, as described in this paper. The FPGA implementation was used to validate the design in at-speed tests in a complete signal emulation system.

Architecture

JPIC performs image compression based on JPEG 2000 [3]. The compression is either lossless or lossy. In the lossy mode, the compression ratio may be defined for each compression session and contained in data headers. Each JPIC requires two 256Mbit SDRAM chips and can receive input via either one or two SERDES chips as in Figure 1. The figure demonstrates a typical JPIC system and the internal structure of the JPIC chip.

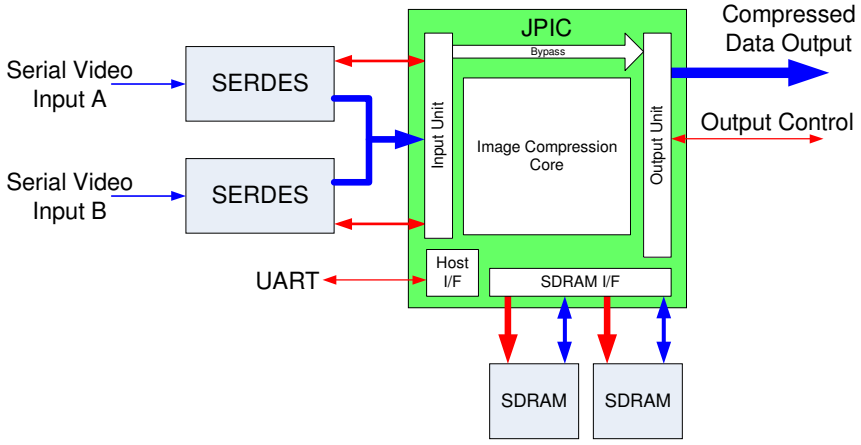

Figure 1: Image compression system architecture

Image data are input to JPIC from either Serial Video Input A or B. JPIC supports input of 10 to 12 bit component data. It can process images at a peak rate of up to 44 Msamples/sec (39MSamples/sec sustained rate). The 24-bit Compressed Data Out delivers standard JPEG2000 files compatible with KAKADU JPEG2000 software [www.kakadusoftware.com]. The Compressed Data Out Control asserts a flag when data are ready at the JPIC output. It manages the writing of Compressed Data Out and enables output multiplexing when multiple JPIC chips share an output data bus. The output is produced at up to 44Mwords/sec. The 1Mbaud UART port allows control and monitoring of the JPIC ASIC. Parameters such as compression rates, lossy / lossless compression and bypass without compression are sent from the host. JPIC also enables system test with built-in synthetic image generation. When no image data is available for compression, JPIC enters a power down mode automatically.

The JPIC ASIC contains 224 SRAM memory cores totalling 5M bit. All memory cores are SEU-protected by EDAC. The ASIC also contains some 300,000 gates. A typical system (Figure 2) may combine multiple JPIC units and multiplex their outputs as they are transferred to storage. Multiple JPIC units can be controlled by a single host (Controller).

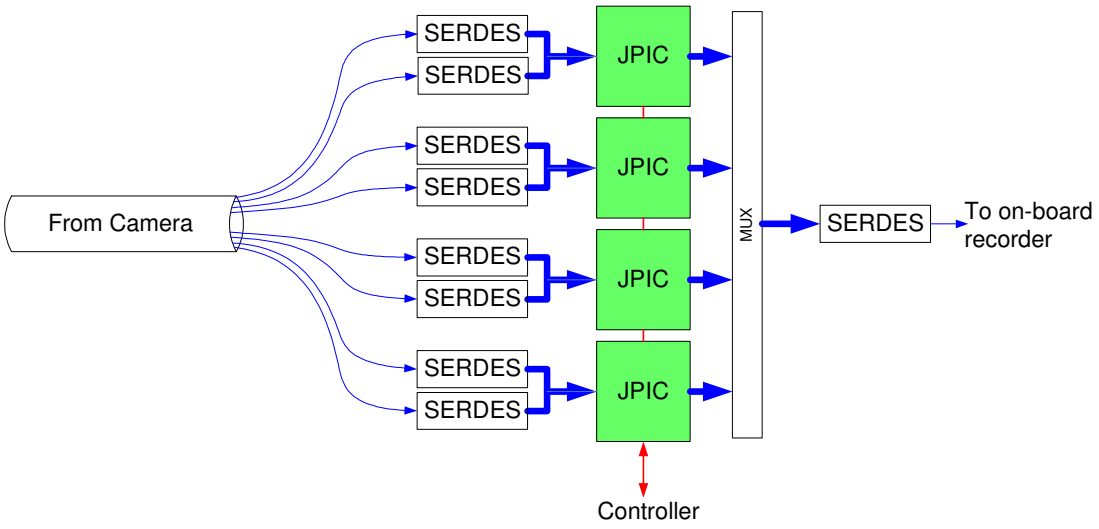

Figure 2: Image compression system using multiple JPIC units

Device characteristics

The device will be manufactured by Tower Semiconductors Ltd. using standard 180 nm CMOS process and packaged in 208-pin 0.5 mm pitch PQFP. It is designed for 1.8/3.3V supplies, Class S temperature range, TID of at least 300 krad (Si), no latchup, cross section below 20μ^2 for SEU (all SRAM cores are EDAC protected and all FFs are SEU-protected), maximum clock frequency of 88 MHz, and maximum power dissipation below 3W.

Conclusions

Collaboration of MBT (a systems company), Alma Technology (an IP core vendor) and Ramon Chips (a RH ASIC design company) yielded JPIC, a rad-hard JPEG2000 image compression chip in both ASIC and FPGA formats.

References

[1] ISO/IEC 15444 Information Technology JPEG 2000 Image Coding System
[2] JPEG2k-E 3H08NM00 - JPEG 2000 Encoder Core – design specification, ALMA Technologies
[3] JPIC Rad-Hard JPEG2000 Image Compression ASIC for Aerospace and Military Markets, Ramon Chips Ltd.