RC64 Radiation Hardening Methodology

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***Abstract* – RC64 is a manycore DSP/CPU for space applications. Chip size is 354 mm2 with ~600M transistors. It is fabricated using 65nm CMOS technology. It integrates 64 DSP cores, ~74Mbit of SRAM bits, 12 6Mbps SERDES ports, DDR2/3 interface to external memory, and a wide LVDS based bus. The chip is assembled in PBGA package, and qualified and screened per space standards.**

The ASIC design methodology is based on a set of guidelines and custom library cells, for hardening it for radiation. The key elements of the Radiation Hardening By Design (RHBD) methodology and Radiation Hardening By Software (RHBS) are described here.

RHBD of SEU is implemented by hardened flip-flops, glitch filtered high fan-out nets, EDAC and interleaving of mitigation of SRAM errors, and error correcting of data from external memory. SEL is mitigated by hardening the SRAM cores, and fixing the hard IPs, provided by IP vendors. RHBS is supported by Fault Detection, Isolation and Recovery (FDIR), error counters, and self-recovery from SEFI.

1. INTRODUCTION

RC64 [1] was processed with standard 65nm CMOS process. It is packaged in 35×35mm 650L PBGA, and the die is ready for assembly in 32×32mm 624L PBGA, CLGA or CCGA.

The digital cell library is based on vendor's standard cell. However, in order to harden the library for SEU and SET, we replaced the more sensitive cells, such as flip-flops, with customized hardened cells.

RC64 requires several hard IPs, including SRAMs, PLLs, DDR2/3 I/F and SERDES. We used proven IPs from leading vendors, and hardened them without affecting their performance. The SRAMs were replaced by "wrappers", which included ECC bits, ECC generator logic, and Error Detection And Correction (EDAC) logic.

The design flow of logic and physical synthesis was modified for enhancing the immunity to SEU and SET effects. For example, critical flip-flops, like configuration and test logic, that might cause Single Event Functional Interrupt (SEFI), were synthesized using highly protected flip-flops, while the rest were synthesized to moderately protected flip flops.

A brief description of the content of RC64 die is presented in Table 1. The layout of the chip is shown in Figure 1.

Die size	354 mm^2
Number of transistors	~600 M
Number of logic gates (equivalent)	~38 M
Number of flip-flops	~2 M
Number of SRAM cores	2830
Number of SRAM bits	~74 M
Number of SERDES cores	12
Number of DDR2/3 cores	1 (48 data bits)
Number of PLL cores	2
Number of I/O pins	272
Number of LVDS/CMOS buffers	83
Number of SSTL buffers	96
Number of PTAT cells	1

Table 1: Content of RC64 die

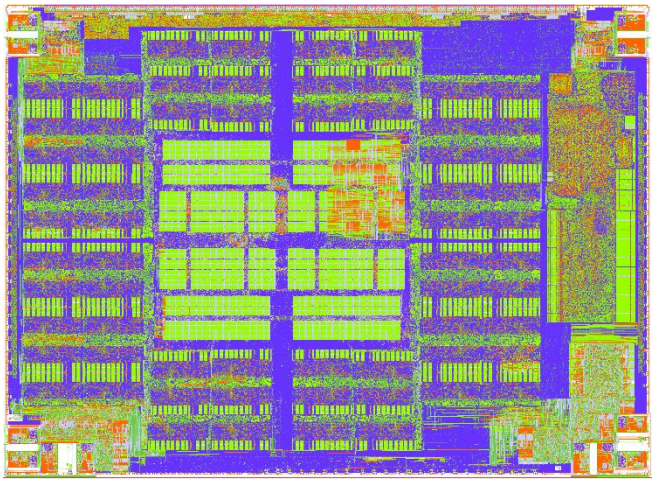

Figure 1: Layout plot of RC64

The hardware protection mechanisms integrated in RC64 include: protecting SRAMs with EDAC, while interleaving sub-words; using DICE-like and Dual Modular Redundancy (DMR) flip flops and latches; Glitch filtered high fan-out logic trees and using synchronous reset [2]; The DDR2/3 I/F is 48-bit wide, to support Error Correction Code (ECC) bits in the external memories, and on-chip EDAC, for correcting

the errors in external memories. The SERDES I/F utilizes SpaceFibre [3,4], a fault tolerant serial communication protocol for space applications. Hardening to soft errors is complemented by several optional software protection procedures, as part of Fault Detection, Isolation and Recovery (FDIR).

In order to enable a wide range of I/O options and various system configurations, while minimizing pin count, we developed a multi-purpose I/O cell, which is configurable as LVDS or CMOS buffer, with configurable direction.

The immunity of the technology and the IP cores was assessed by development of a test chip containing all the hard IPs, and performing radiation testing of Total Ionizing Doze (TID), Single Event Latch-up (SEL) and Single Event Upset (SEU) for each IP separately. The lessons learned during that experiment were implemented in the final product.

2. RADIATION HARDENING BY DESIGN (RHBD)

This chapter describe the main concepts used for hardening the RC64 to all radiation effects.

For assessing the immunity of all the hard IP cores of the RC64 to all radiation effects, we developed a test chip, and tested it for radiation effects. It enables us distinguishing between the sensitivities of each circuit exclusively, and enables us to qualify the IP cores and refine the methodology. The radiation tests had been done by Soreq, nuclear research center, Israel, while the SEL and SEU tests where done in CYCLONE - Heavy Ion Facility (HIF) in Belgium.

Immunity to TID

Measurements done on the test chip after stressing the device at 300Krad from Co^{60} source, indicated that the random logic are fully immune to TID. For example, the frequency of the ring oscillator was not changed, as can be seen in Figure 2.

The SRAMs are immune to TID. Measurements of the impact of TID on the SRAM, done on the test chip, indicate that there is a negligible increase of supply current up to 100Krad, and very minor increase of current at 300Krad, which is equivalent to <20mA for the entire chip.

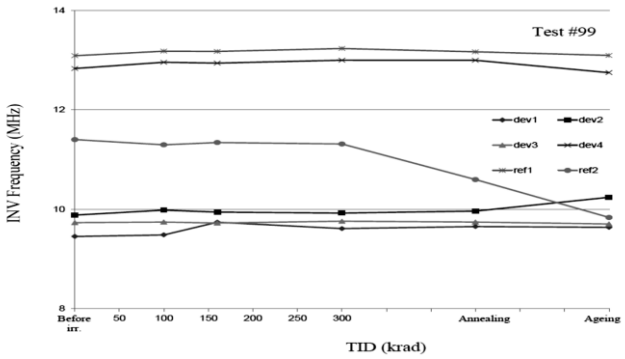

Figure 2: Impact of TID on frequency of ring oscillator

The hard IP cores (SERDES, DDR2/3), are proprietary of the IP vendors. We had hardened the layout of these cores for TID and SEL by adding guard rings all over, in such a way that it will not affect the performance of the cores.

Mitigation of SEL

Measurements done on the test chip, using high energy ions, while the device is operating at maximum specified voltage and temperature provided the following results: No SEL induced current observed on the random logic, I/O cells, and hard IP cores. However, measurements of the SEL of the large memory SRAM modules indicated that they demonstrated some "soft latch-up". Tests are done at maximum supply voltage, and junction temperature of 125°C while stressing the devices with Xe ions with effective LET of 62.5 MeV*cm^2/mg. The term "soft latch-up" means that latch-up events increase the supply current by up to few tens of mA at each event. This current did not cause permanent damage, but accumulation of such events might stress the power grid and increases the total power. Using DNW under the entire core, as proposed in [5,6], increases the SEL rate.

In order to protect the SRAMs from SEL, we implemented a fixing the SRAMs in such a way that the immunity to SEL improved significantly. The characterization of the SEL immunity will be done soon.

Mitigation of SEU in flip-flops

In the test chip, we had evaluated the SEU rate for various types of flip-flops, including DICE-like [7], DMR, TMR and reference flip-flop from vendor's library. The concept of the DMR flip-flop used is described in Figure 3.

The DICE-like flip-flops demonstrated SEU rate of >20X better, and the SEU rate of DMR flip-flop is >1000X better than the reference vendor's flip-flop.

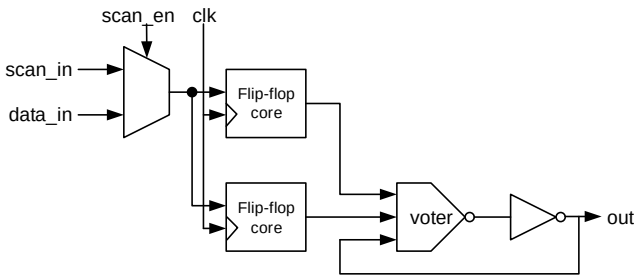

Figure 3: Concept Dual Modular Redundancy (DMR) flip-flop

We had sorted the flip-flops in the chip per their criticality. The most critical flip-flops are those used for configuration registers, test logic, control logic and state machines. For these flip-flops, we used DMR flip-flops and additional levels of protection. The rest of the logic is based on DICE-like flip-flops. The clock gators, which have latches inside, are protected by TMR latches.

Flip-flops with asynchronous set or reset are also sensitive to SET of their asynchronous inputs. We used synchronous reset in most of the chip. However, few cases require asynchronous reset.

Mitigation of SEU in SRAMs

SEU of all the SRAMs was mitigated by adding Error Correction Code (ECC) and Error Correction And Detection (EDAC) logic. We compiled the SRAM to have maximum multiplexing ratio, thus maximizing the distance between the bits of the same logic word. However, since the physical distance between the bit cells of the same logic word are placed within ~8u from each other, a single heavy ion might cause Multi Bit Upset (MBU), which is not correctable by a regular EDAC logic. We had detected, when testing the SRAMs of the test chip, up to 3 flipped bits per word when using Xe ions, with 62.5 MeV*cm^2/mg and vertical inclination.

For mitigating this effect, we split each word in the SRAM to several interleaved sub-words, and implemented the ECC and EDAC to each sub-word. This method increased the number of physical bits, but mitigated potential uncorrected SEU caused by MBU by single ion. Figure 4 demonstrate the implementation of the interleaving, in case of interleaving by two.

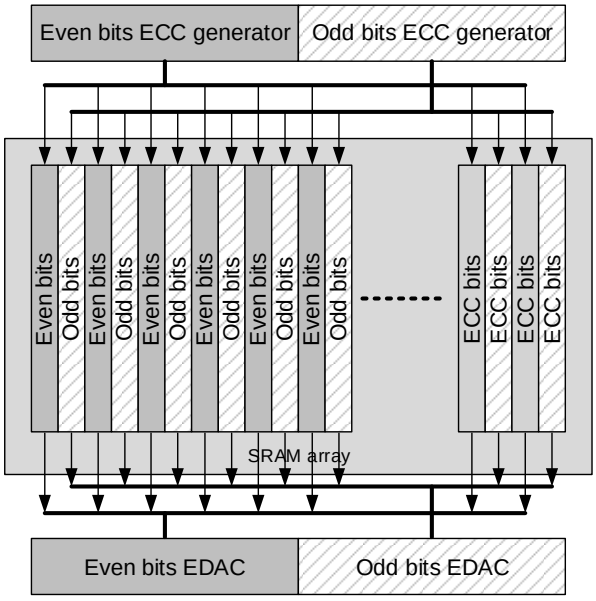

Figure 1: Concept of interleaved ECC+EDAC for MBU/SEU mitigation in dense SRAMs

Mitigation of SEU in external memories

RC64 employs Reed-Solomon (R-S) ECC for DDR2/3 external memories. 16-bit ECC is appended to each 32-bit word. The 48 bit word is interfaced to six DDR2/3 byte-wide devices. The R-S code facilitates correcting bit errors, as well as recovery from SEFI of one of the DDR2/3 devices.

Mitigation of SET in high fan-out nets

High fan-out nets are signals that propagate from a single node, typically for configuration or control bit, and spread to many destination nets. Since there is a need for many stages of buffering, a Single Event Transient (SET) event in any of the buffer stages of this net might trigger a spike that is affecting many circuits. Such spike might cause major logic error or SEFI. These nets include the *reset*, *scan_enable*, *block_enable* and configuration signals. Typically, these nets have default logic state for the normal operation mode, and alternative state for testing, initialization and other rare events.

We had implemented special buffers for these nets, that is narrowing the input pulses relative to the default logic state, thus filters narrow glitches, generated by SET events. The concept of such buffer with normally low signals is described in Figure 5.

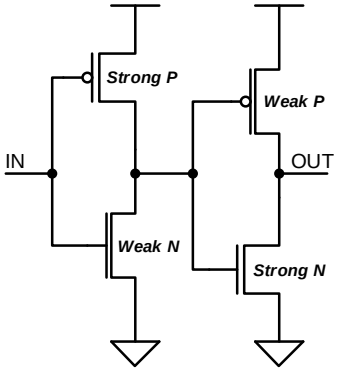

Figure 2: Schematic of normally-zero glitch filtering buffer used for high fan-out nets

3. SPECIAL I/O CELLS

PTAT temperature sensor

The device is designed to operate and be tested at extreme temperatures. Since placing a temperature sensor on the package is not always possible, we designed an on-die temperature sensor. It is based on a Proportional To Absolute Temperature (PTAT) circuit, implemented by CMOS devices only. It generates current that is linearly proportional to absolute temperature, independent on supply voltage and process parameters. This current can be measured off-chip, and can be used for continuous monitoring the die temperature.

LVDS/CMOS I/O buffer

The RC64 is designed to support several interfacing protocols, which require either LVCMOS or LVDS signals, in both directions. We implemented multi-function I/O pads, in order to reduce the total number of pads.

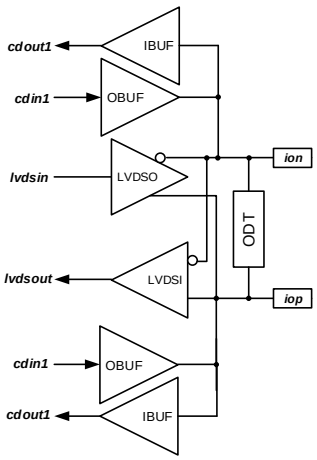

Figure 3: Configurable LVDS/CMOS bi-directional I/O buffer

The schematic of the buffer is described in Figure 6. The two external pads can be used either as: Two LVCMOS inputs with optional pull-up/down and hysteresis; Two LVCMOS outputs with configurable drive strength; LVDS input with configurable On-Die Termination (ODT); LVDS output with configurable drive strength. The LVCMOS buffers can operate at I/O supply voltage of 1.6÷3.6V. The LVDS can run up to 800Mbps (400MHz).

4. RADIATION HARDNESS BY SOFTWARE (RHBS)

In addition to the RHBD methods, the RC64 support several complementary software driven techniques for monitoring the soft errors and mitigation soft errors and Single Event Functional Interrupt (SEFI). The following are the key RHBS features and concepts supported by RC64.

Fault Detection Isolation and Recovery

RC64 implements extensive means for fault detection, isolation and recovery. An external host can reset, boot and scrub the device through dual SpaceWire ports.

Error counters

RC64 contains error counters and monitors that collect and report error statistics. Trace buffers, allocated in shared memory enable tracing back the error events for easing the debug.

Watchdog

Internal programmable timers can be programmed to reset the chip after a specific timeout period, thus self-recovering SEFI events. In such event, the host is informed, thus enabling monitoring such events.

5. CONCLUSIONS

RC64 is a high performance, many core DSP suitable for use in space. It enables a wide range of applications, while providing high level of protection from radiation effects.

RHBD is implemented by hardening the licensed IPs cores, enriching the cell libraries with additional cells, and adding error correction logic to internal and external memories.

In addition, RHBS techniques, based on on-chip error monitors, enable error mitigation and self-recovery from SEFI.

A configurable IO buffer supports interfacing with peripheral devices by several optional interfaces at high data rates. An on-die temperature sensor helps to monitor junction temperature in all environments.

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